Control-Hardware-in-the-Loop Study of Islanding: 3V0 and 3I0 Events

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Control-Hardware-in-the-Loop Study of Islanding: 3V0 and 3I0 Events

Final Report

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Abstract

The development of the methodology in this project for a control-hardware-in-the-loop (CHIL) real-time simulator provides a platform for better comprehension and evaluation of the critical issues unique to New York State electric systems. The methodology can be readily applied to assess impacts on electric systems from which the industry can build knowledge for specifying requirements for interconnecting distributed energy resources (DER). Simple simulation has not been sufficient to evaluate certain phenomena and limits the ability to assess the effectiveness of proposed solutions for DER. Reasons for the insufficiency include (1) the lack of readily available and accurate simulation models of manufactured equipment and (2) basic testing of individual equipment does not capture the more serious effects of interaction among different types of devices connected to the same feeder. A real-time CHIL simulation model, as demonstrated in this study, presents a method which addresses these deficiencies and provides another tool for resolving DER interconnection issues. To demonstrate the approach and methodology for CHIL simulation, models for three operating distribution feeders were developed and connected to two inverter controllers of different ratings. The setup was put together at the test facility at Rensselaer Polytechnic Institute (RPI) and interconnected with the OPAL-RT simulator,[1] a software that enables the key functions of CHIL simulation. The following results and findings are specific to the studied feeders and inverters.

- **Unintended Islanding**. In the study, the inverters tested use an alternating pulse in inverter current with constant time period. The tests showed that the inverters trip within two pulse periods, or at most 1.93s. The slower trip times for an inverter apply to certain system conditions, including (a) presence of another inverter on the circuit, (b) the inverter is located on the remote end from the feeder breaker, and (c) it is on a feeder with no capacitor bank. Even when two inverters use similar methods for active anti-islanding detection with the same pulse period, their response times to an islanding event can be dissimilar. In the tests, the larger inverter tends to trip faster than the smaller inverter regardless of feeder type and configuration, location of the inverters on the feeder or whether or not another inverter is on the feeder. There is an apparent delay in trip time when two inverters are on the feeder compared to when there is only one, but the delay is no more than the time to incur an extra pulse or half a pulse period. All the tests conducted had all connected inverters tripping within the 2s limit on response time specified in Institute of Electrical and Electronics Engineers Standard (IEEE Std)-1547. When active anti-islanding is disabled or not available, the inverters fail to trip within 2 seconds. Remedial measures, such as direct-transfer trip (DTT), are needed for this situation.

- **Ground Fault Overvoltage (GFOV) on the Subtransmission Line**. Since a GFOV event involves an islanded system, albeit with a single line to ground fault (SLGF), the anti-islanding protection of the inverters play a role on whether or not the inverters will trip. For the inverters considered in the study, when active anti-islanding is enabled, even for a fully balanced island, the inverters trip within the same time frame as noted in the islanding test. This duration may be long enough to affect equipment. New York State utilities indicate that the longer trip times, up to 1.93s, is an unacceptable duration for GFOV as it poses a safety risk to personnel. For faster trip times, remedial measures, such as 3V0 and the negative-sequence voltage (NSV) protection schemes, are needed for this situation. The NSV protection scheme will be able to detect the incipient GFOV condition and trip the inverter at a much faster response time than the 3V0 scheme.
- **Ground Fault Overvoltage (GFOV) on the Distribution Feeder**. The simulations show that the voltages remain within normal operating range and no GFOV is observed.
- **Ground Fault Over Current (GFOI)**. When there is an alternate grounding source on the same sub-transmission system, GFOV is not likely to form. However, there is a ground fault current that flows in the alternate grounding source. The magnitude of the 3I0 current in the transformer is less than its continuous rating per American National Standards Institute (ANSI)/IEEE Std. 32-1972 and significantly less than the short-term rating. There is, therefore, not enough ground fault current to overload the transformer.

The development of the methodology for a hardware-in-the-loop real-time simulator provides New York State utilities with a platform for conducting simulations of specific distribution feeders and circuits, embedding actual proposed hardware and trying out potential mitigation options.

Keywords

Islanding, ground fault overvoltage, 3V0, GFOV, ground fault overcurrent, 3I0, inverter-based distributed generation, photovoltaic generation, single-line-to-ground fault, PV, anti-islanding, control-hardware-in-the-loop, CHIL

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Acronyms and Abbreviations

3V0	Three times of zero sequence voltage. 3V0 overvoltage is an indicator for ground fault overvoltage
CESIR	Coordinated Electric System Interconnection Review
DER	distributed energy resources
DG	distributed generation
DPS	Department of Public Service
EPS	electric power system
GFOC	ground fault overcurrent
GFOV	ground fault overvoltage
high side	High-voltage side f the substation transformer. May include the sub-transmission line that connects to the high-voltage side of the transformer.
CHIL	Control-hardware-in-the-loop simulation
HV	high voltage
HV breaker	Circuit breaker located at the sending end of a sub-transmission line
IEEE	Institute of Electrical and Electronics Engineers
IGBT	insulated-gate bipolar transistor
ITWG	Interconnection Technical Working Group
kA	kilo amperes

km	kilometers
kV	kilovolts
kVAR	kilovars
kWh	kilowatt hours
LCL harmonic filter	Type of harmonic filter used in inverters
low-side	Low-voltage side of the substation transformer. May include the feeders connected to the low-voltage side of the transformer.
LFRT	low frequency ride-through
LVRT	low-voltage ride-through
mi	miles
ms	milliseconds or one thousandth of a second
m/s	meters per second
MPPT	Maximum Power Point Tracking
MW	megawatts
NREL	National Renewable Energy Laboratory
NYS	New York State
NYSEG	New York State Electric & Gas, a wholly-owned subsidiary of AVANGRID, Inc.
NYSERDA	New York State Energy Research and Development Authority
Ω	ohm, unit of measurement for electrical resistance
Phase 1 Study	Prior study documented in “Assessment of Inverter-based Distributed Generation Induced Ground Fault Overvoltage on Delta-Wye Substation Transformer”, Pterra Report R149-16 dated 3 January 2016
PSCAD	PSCAD™/EMTDC™ software developed by the Manitoba HVDC Research Center
PU	per unit, normalized electrical units
PWM	pulse width modulation
PV	solar photovoltaic power plant
RMS	Root-mean-square, a method for representing repeating sinusoidal signals as an average value
RPI	Rensselaer Polytechnic Institute
s	seconds
SIR	Standard Interconnection Requirements as documented in “New York State Standardized Interconnection Requirements and Application Process for New Distributed Generators 5 MW or Less Connected in Parallel with Utility Distribution Systems,” New York State Public Service Commission
SLG	single-line-to-ground, descriptive for a type of fault or short-circuit
Substation Transformer	Refers specifically to distribution transformer connecting the sub-transmission voltage equipment and facilities with distribution voltage level feeders and circuits

TOV	temporary overvoltage
µs	microsecond or a millionth of a second
UL	Independent laboratory that certifies, validates, tests and verifies PV inverters
W	watts
Ygrounded	wye-grounded connection of a transformer

Summary

The development of the methodology in this project for a control-hardware-in-the-loop (CHIL) real-time simulator presents a platform for better comprehension and evaluation of the critical issues unique to New York State systems. The methodology can be readily applied to assess impacts on electric systems from which the industry can develop knowledge for specifying requirements for interconnecting distributed energy resources (DER). The specific issues demonstrated in this study relate to those issues which have been shown to have delayed the assessment and approval of interconnection projects of DER in New York State, that is, unintended islanding, ground fault overvoltage (GFOV) and ground fault overcurrent (GFOI). The approach and methodology demonstrated in this study may also be amenable to other technical issues.

As the industry develops an understanding of the many complex issues associated with the integration of DER, it has not been sufficient to use an all-computer-simulation approach to evaluate these phenomena and the proposed potential solutions. For one, accurate simulation models of manufacturer equipment are not readily available. Nor is basic testing of individual equipment sufficient, as the interaction effect of different types of devices is not captured. Real-time simulation using actual control hardware, as used in this study, presents a method that addresses these deficiencies and helps resolve DER interconnection issues by embedding actual proposed hardware and trying out potential mitigation options.

To demonstrate the approach and methodology for CHIL simulation, three operating distribution feeders were modeled, and two inverter controllers of different ratings were obtained from the manufacturers. These were put together at the test facility at Rensselaer Polytechnic Institute (RPI) and interconnected with the OPAL-RT simulator,[2] a software that enables the key functions of CHIL simulation. The following results and findings are specific to the studied feeders and inverters. Any conclusions inferred herein are specific to the study cases and may not generally be applicable to all feeders and inverters. Non-inverter-based DER may have significantly different responses and are not covered in the study.

S.1 Unintended Islanding

- Inverters use different methods for active anti-islanding protection. In the study, the inverters introduce an alternating pulse with constant pulse duration, T_p, and period, T_d. Even when two inverters use similar methods for active anti-islanding detection with the same pulse width and period, their response times to an islanding event are dissimilar as evidenced by the different standard deviations of trip time, T_t, between the two inverters used in the tests.
- The inverter trip time is a function of when the islanding occurs in relation to the point in time within the inverter pulse period. If an islanding event occurs immediately after a detection pulse, the inverter takes just a little more time to detect the island compared to an event which occurs just before a pulse. In the case of the of the study inverters, the trip times can vary but remain within a specific number of pulses, that is, 1–2 pulses represent a time range of 0 to 0.965s; 2–3 pulses create a time range of 0.483 to 1.448s, and 3–4 pulses produce a time range of 0.965 to 1.93s.
- There is an apparent delay in trip time when two inverters are on the feeder compared to when there is only one, but the delay is no more than the time to incur an extra pulse.
- For cases with two inverters on the feeder, once the first inverter trips, the remaining inverter trips not only on its own active anti-islanding protection but may also trip on its passive anti-islanding function since the feeder conditions will now show unbalanced voltage and frequency.
- When active anti-islanding is disabled or not available, the inverters fail to trip within 2 seconds. Remedial measures, such as direct-transfer trip (DTT), are needed for this situation. The DTT should initiate on the opening of the feeder breaker and send a trip signal to the inverter(s).
- When the study inverters' active anti-islanding protection is enabled, the 1000-kilowatt (kW) inverter tends to trip within 1-3 pulses regardless of feeder type, location in the feeder, or whether or not another inverter is on the feeder. The 500-kW inverter has a slower response requiring at least two pulses and, in some cases, up to 4 pulses (when two inverters are on the feeder). All the tests conducted had all connected inverters tripping within the 2s limit on response time specified in Institute of Electrical and Electronics Engineers Study
(IEEE Std)-1547.
- The slower trip times for an inverter apply to certain system conditions, including (a) presence of another inverter on the circuit, (b) the inverter is located on the remote end from the feeder breaker, and (c) it is on a feeder with no capacitor bank.

S.2 Ground Fault Overvoltage on the Subtransmission Line

- Since a ground fault over overvoltage (GFOV) event involves an islanded system, albeit with a single line to ground fault (SLGF), the anti-islanding protection of the inverters can play a role on whether or not the inverters will trip. For the inverters considered in the study, when active anti-islanding is enabled, even for a fully balanced island, the inverters trip within the same time frame as noted in the islanding test, anywhere from 1 to 4 pulses. The time to trip the inverters and de-energize the island can be as much as 1.93s. This duration may be long enough to affect equipment. New York State utilities indicate that this is an unacceptable duration for GFOV as it poses a safety risk to personnel.
- The CHIL tests confirm that following the SLGF and formation of the island, voltages as high 1.75 times the pre-event values are observed on the high side of the substation transformer and on the subtransmission system. This is consistent with the all-software simulation (from the Phase 2 Study).
- When the active anti-islanding feature is disabled, the inverters do not trip for a fully balanced island, indicating that passive anti-islanding is unable to detect the presence of the ground fault on the subtransmission line. If left undetected, the GFOV can remain active for as long as balanced conditions are present on the island.
- Two remedial measures were evaluated. For faster trip times, remedial measures, such as 3V0 and the negative-sequence voltage (NSV) protection schemes, are needed for this situation.
    - New York State utilities require the implementation of a 3V0 protection. This scheme requires additional equipment and construction at the utility substation that can be expensive for developers of inverter-based generation and will also impose a time delay to their projects. The 3V0 scheme will wait until the sensing relay detects the overvoltage and sends a trip signal to the feeder breakers. This could take as long as 6-24 cycles (0.1 to 0.4 seconds) to occur, just a little bit faster than active anti-islanding protection. In the meantime, the overvoltage remains on the high voltage side.
    - For the NSV protection scheme, the response is based on the sequence voltages. The NSV protection scheme will be able to detect the incipient GFOV condition and trip the inverter at a much faster response time than the 3V0 scheme.
- For the specific inverters tested here, the inverter trip occurs due to the anti-islanding protection. These particular inverters do not detect the overvoltage, unlike some simulation models that were studied previously. Other types and designs of inverters may be able to trip faster by detecting the overvoltage event or by using shorter anti-islanding detection cycles or other forms of anti-islanding protection.

S.3 Ground Fault Overvoltage on the Distribution Feeder

- This tests for ground fault overvoltage (GFOV) following a SLGF fault at the inverter terminal. However, the simulations show that the voltages remain within normal operating range and thus no GFOV is observed.

S.4 Ground Fault Over Current

- When there is an alternate grounding source on the same sub-transmission system, ground fault over current (GFOV) is not likely to form. The alternate grounding source is generally in the form of a customer transformer with a wye-grounded/delta connection, a three-winding transformer or an autotransformer. However, there is a ground fault current that flows in the alternate grounding source. For the simulations, the magnitude of the 3I0 current in the transformer is less than its continuous rating per American National Standards Institute (ANSI)/IEEE Std. 32-1972 and significantly less than the short-term rating. There is, therefore, not enough ground fault current to overload the transformer. No mitigation is required since the transformer can withstand the GFC in this scenario.

S.5 Concluding Statement

The present report presents the research and findings for what is essentially Phase 3 of a multiphase GFOV and islanding study proposed to New York State Energy Research and Development Authority (NYSERDA) by Pterra LLC.

Phase 1 of the study was an initial assessment of the GFOV phenomena using software simulation. The results of Phase 1 are documented in the report titled, Assessment of Inverter-based Distributed Generation Induced Ground Fault Overvoltage on Delta-Wye Substation Transformer, Pterra Report R149-16 dated 3 January 2016.[3] One of the findings of the Phase 1 study is that GFOV energized by inverter-type distributed generation (DG) can occur under specific system conditions and equipment configurations.

Phase 2 of the study had the following objectives: (a) to investigate, using software simulation, the nature and characteristics of the specific form of GFOV that has certain New York State utilities requiring a 3V0 protection scheme of interconnecting DG, (b) to identify or develop an alternative protection method that may not be as onerous in cost and time penalty as the 3V0 scheme, and (c) to provide additional guidance to solar photovoltaic power plant (PV) developers and utilities on how to evaluate for GFOV potential and provide future design options that will prevent or mitigate the GFOV issue. The Phase 2 objectives are met as presented in the report titled Alternate Mitigation and Design Options to 3V0 Requirement, Pterra Report R106-18 dated 2 May 2018. A summary of the report was presented to the ITWG.

This report documents Phase 3 of the study. In the study, simulation models for three distribution systems representative of typical New York State feeders are developed. Instead of computer models of PV inverter controls, actual hardware in the form of control boards are integrated in the same simulation loop as the computer models of the distribution circuits; the overall setup is referred to as control-hardware-in-the-loop or CHIL simulation. This is a demonstration study that establishes the approach and methodology for conducting similar assessments of specific feeder configurations, inverter design, and mitigation options. The procedure presented herein may also be adapted to studying other forms of technical issues.

1 Introduction

1.1 Background

New York State utilities have identified a number of technical issues when evaluating impacts of interconnecting distributed energy resources (DER) on their electric systems. Such issues, where not clearly understood, can lead to delayed assessment and approval of interconnection projects. In specific cases, software simulation has not been sufficient to evaluate these phenomena and any proposed mitigation. For one, accurate simulation models of manufacturer equipment are not readily available or are provided in the form of "black-box" models whose features and functions are not transparent. Another limitation of software modeling is that the interaction of multiple inverter-based DER are not practical to simulate due to incompatibilities between user-models from different manufacturers and the increase in elapsed-time to simulated-time ratio as more user-models are simulated together.

Control-hardware-in-the-loop (CHIL) simulation technology allows a hybrid approach where the known electrical characteristics of distribution feeders and their components can be modeled in software while the unknown, hidden, or actual response of inverter control hardware is captured from the physical control boards. CHIL simulation is real time, that is, the elapsed-time to simulated-time ratio is unity. This facilitates the conduct of testing and study as more test cases can be performed once the initial set up and procedures have been completed.

The overall concept for this project is to demonstrate an approach and methodology that New York State utilities can apply when evaluating impacts on their electric systems. The present scope does not provide for an exhaustive analysis of all the various distribution circuit configurations, load types and power factor, or inverter manufacturer and designs, including anti-islanding schemes, and other salient aspects of interconnecting distributed energy resources (DbER) to feeder circuits. Rather it demonstrates how a select feeder and inverter control boards can be integrated in a CHIL simulation setup to study specific technical issues. The specific issues demonstrated here relate to those which have been shown to have delayed the assessment and approval of interconnection projects of DER in New York State, that is, unintended islanding, ground fault overvoltage (GFOV) and ground fault overcurrent (GFOI). The approach and methodology demonstrated in this study may also be amenable to other technical issues.

The following subsections provide a background on the nature of the three technical issues studied, the concerns which each issue brings in terms of reliability, power quality, equipment protection, implementation cost and personnel safety, and the proposed mitigation as identified during the interconnection process.

1.2 Islanding

The introduction of DER into distribution circuits provides the basis for concerns regarding unintentional islanding (or simply "islanding" as used in the context of this report). Whereas prior to the addition of DERs to a feeder, the event of opening the distribution breaker, for whatever reason, would lead to de-energization of the feeder. The presence of DER may provide enough energy to keep the feeder energized even though islanded from the grid source. Hence, in the context of this study, an "island" means an energized isolated feeder circuit.

Industry studies have identified a number of conditions that can lead to the phenomenon of islanding. A commonly used set of conditions for determining potential for islanding is the Sandia guide, based on Suggested Guidelines for Assessment of DG Unintentional Islanding Risk, a report from Sandia National Laboratories by M. Ropp and A. Ellis, dated March 2013. The guideline specifies two sets of screens that would determine if there is potential risk of islanding. The first screen relates to the balancing of real power on the islanded circuit, that is, when the ratio of inverter-based DER watts to the minimum load watts is small, say less than 0.67, then the DER is unlikely to maintain an energized island. The second screen relates to the reactive power or voltage control on the island, that is, if the reactive supply is not balanced on the island, voltages tend to exceed normal operating limits, which will trigger the DER to trip.

In New York State, the Sandia screen has been adopted into the standardized practice for any DER connecting to the distribution system. This is documented in Unintentional Islanding Protection Practice for Generation Connected to the Distribution System, prepared by the Joint Utilities of New York, version dated February 9, 2017. (In this report, the specifications of the document are hereinafter referred to as the New York Islanding Practice.)

In part as a response to concerns raised with islanding, inverter manufacturers have developed various anti-islanding techniques. There are two forms, passive and active anti-islanding. Passive anti-islanding involves monitoring conditions at the point of interconnection of a DER, typically voltage and frequency, and triggering a trip of the DER when those conditions are not within specified parameters, which would

include time factors and rate-of-change. Passive anti-islanding tends to have a large non-detection zone to avoid nuisance tripping to comply with other standards (such as IEEE Std-1547) or due to lack of sensitivity of the monitoring functions. Active anti-islanding may take many forms which typically involve injecting a disturbance signal and determining from the grid response if an islanding event has occurred. Inverter control designers and manufacturers generally do not reveal their active islanding methods and details and hence the need to actually test specific equipment for their characteristics. It is even more important to then test the interaction of multiple inverter-based DER of different size and design. Furthermore, active anti-islanding schemes' response can vary depending on the specific circuit conditions and configurations.

Despite the industry-wide concern about islanding, there have been remarkably few, if any, reported instances of actual islanding that was long enough to present a concern for personnel and equipment. Many reported instances are apocryphal with scant recorded information to confirm and investigate the causes. The studies in this report look to clarify the islanding issue further by providing a platform for evaluating multi-inverter interactions and testing different types of inverter designs and anti-islanding techniques on different types of feeders.

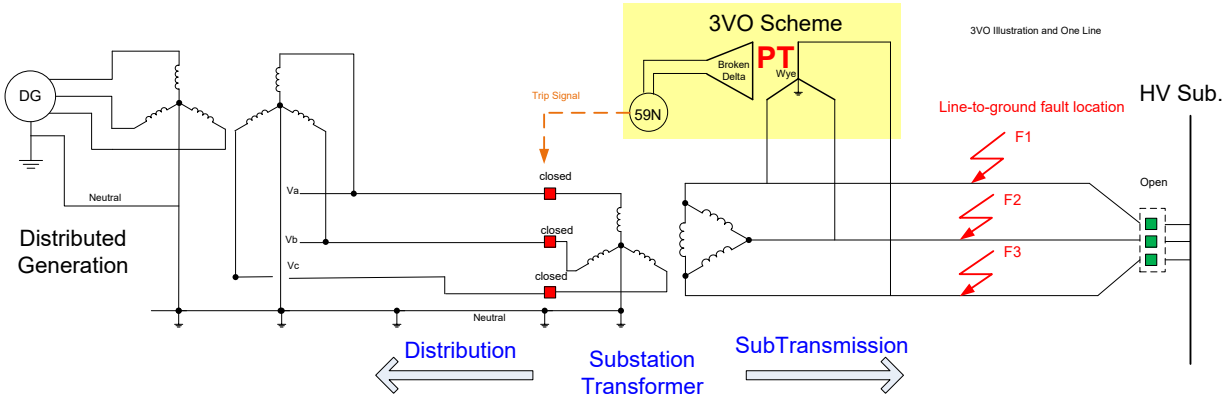
1.3 Ground Fault Overvoltage

Recent interconnection studies for proposed inverter-based solar photovoltaic energy resources identify a potential issue regarding ground fault overvoltage (GFOV). The potential GFOV occurs under certain electrical configurations which are subject to a specific sequence of events, described in further detail below. A utility in New York State that encountered the issue in the course of evaluating a PV interconnection application, required the implementation of a protection scheme based on measurement of zero sequence voltage[4] (referred to simply as a 3V0 scheme[5]).

GFOV can arise under certain electrical configurations (such as when the ratio of the DER to load on the feeder is high or when the inverter anti-islanding protection fails to detect the faulted island)[6] which are subject to a specific sequence of events. Figure 1 shows the typical configuration. The inverter-based PV applying to interconnect to the distribution system is designated as DG on the left side of the figure. There may be other customers and other DG connected to the same distribution feeder but are not shown in the figure. The substation transformer is specifically configured as two-winding connected delta on the high (or sub-transmission) side and wye-ungrounded on the low (or distribution) side. A sub-transmission line connects the high side of the substation transformer to a remote high-voltage (HV) substation. Circuit breakers (non-grounding type) are provided on the HV substation side of the sub-transmission line, but

not on the distribution substation side. These breakers are hereon referred to in this report in the singular as "HV breaker." (Before the addition of DER to the distribution feeders, the sub-transmission line functioned as a radial feed to the distribution load hence only one set of circuit breakers is provided, located on the sending end of the line represented by the HV substation.)

Figure 1. Electrical Configuration for GFOV and 3VO Scheme



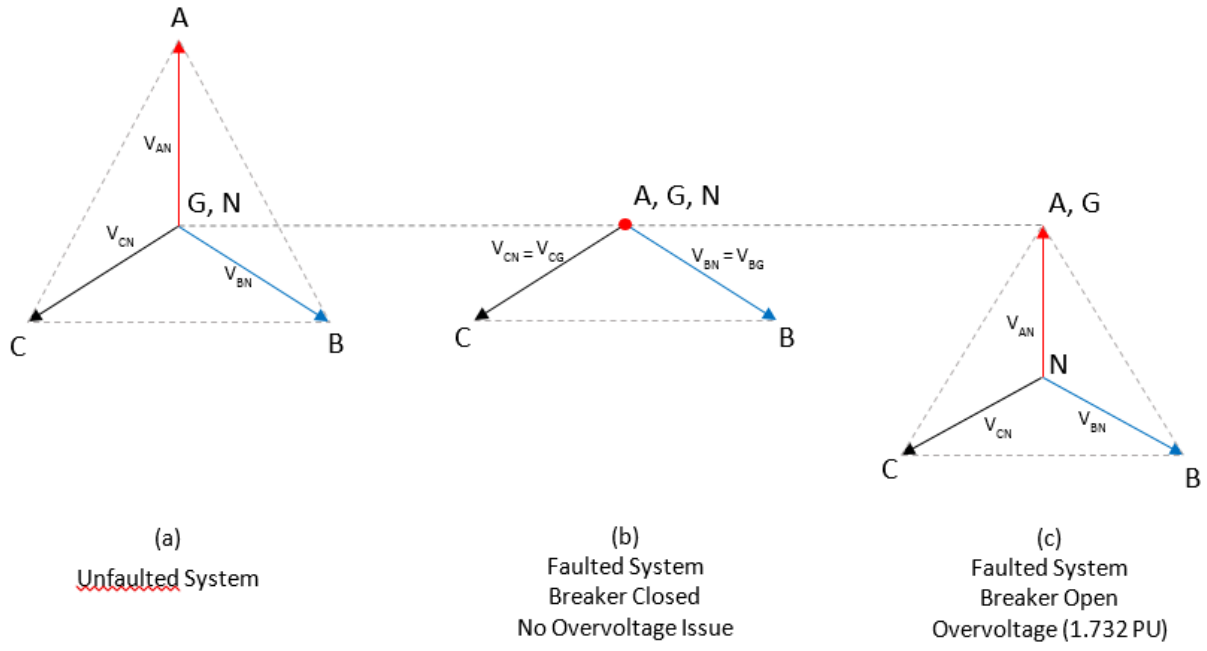
For the configuration shown in Figure 1, GFOV can arise on the following sequence of events:

1. A solid or low-impedance, single-line-to-ground (SLG) fault occurs at any of the locations F1, F2, or F3.
2. The fault is detected by the sub-transmission protection, which then trips the HV breaker. This islands the sub-transmission line and connected distribution feeders. Normally, the island will de-energize if all the connected facilities are typical customer loads.
3. With sufficient amount of DER on the island, the island may stay energized with the fault still present. Other protection on the island, including those provided with the DER, particularly, inverter-based PV, may fail to detect the fault and islanded condition, or the protection may detect the islanded condition but allow it to remain energized for a certain duration.
4. A form of temporary overvoltage (TOV), known as a ground fault overvoltage (GFOV), then arises on the sub-transmission segment of the island. The duration that the GFOV remains can potentially be long enough to pose a safety risk to personnel and/or damage electrical devices and equipment.

Figure 2 shows the phasor diagram for the sub-transmission voltage under various stages of the above sequence of events. In (a), before the SLG fault occurs, the three phase voltages are nominal at 1.0 per unit (PU). In (b), the SLG fault occurs on phase A, but the breaker at the HV substation has not yet opened. Here, voltage on the grounded phase is, at worst, zero, hence, $V_{AN} = 0$, while the unfaulted phases remain nominal, hence, $V_{BN} = V_{CN} = 1$ PU. In (c), HV substation breaker has opened. Here, the sub-transmission voltage no longer has a grounding source which causes the neutral point, N, to shift.

Now, the voltage on the unfaulted phases are $V_{BG} = V_{CG} = 1.732$ PU. This high voltage is what is referred to as GFOV. The GFOV remains in place as long as there is excitation from the low side of the substation transformer and lightning arresters do not start to conduct.[7] Furthermore, actual GFOV will have transient and non-fundamental components with complex waveshapes.[8]

Figure 2. (a) Voltages Prior to Single-Line-to-Ground Fault (SLG) on Phase A, (b) During SLG with Breaker Close, and (c) During SLG with Breaker Open



(a) Unfaulted System

(b) Faulted System Breaker Closed No Overvoltage Issue

(c) Faulted System Breaker Open Overvoltage (1.732 PU)

Since the voltage on the low side, where the inverter-based PV are connected, remains normal with the SLG fault still connected and after the HV breaker has opened, the connected DER may not recognize that there is a GFOV event on the high side. As noted in the report Alternate Mitigation and Design Options to 3V0 Requirement, Pterra Report R106-18 dated 2 May 2018 (hereinafter referred to as the "Phase 2 Report"), containing the software simulation study that preceded this present study, some manufacturer simulation models are able to recognize either the islanded condition or the presence of a fault and do trip the DER, while others do not and stay online, continuing to energize the GFOV. Due to this uncertainty in the actual response of inverter-based DER, New York State utilities require mitigation in the form of an additional protection scheme, the 3V0 scheme.

The 3V0 scheme is shown in Figure 1, highlighted in yellow. It is connected to the sub-transmission side of the substation transformer via potential transformers (PT). The measured 3V0 voltage, triggers a ground fault overvoltage relay (device 59N), which then provides a trip signal to the breakers on the distribution side of the substation transformer.

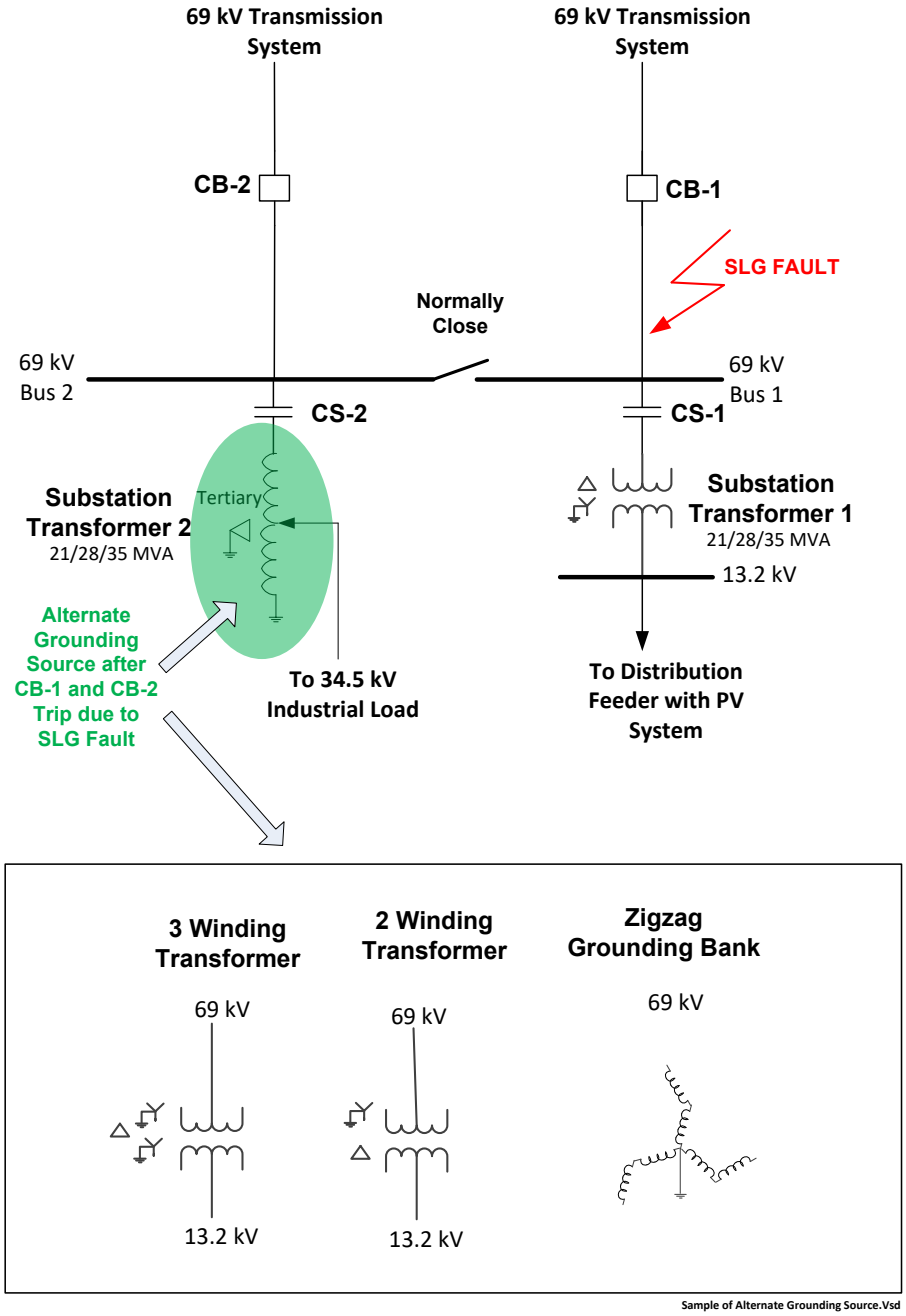
In the Phase 2 Report, an alternative protection scheme was posited, designated as the Negative Sequence Voltage (NSV) scheme. Using software simulation, it was demonstrated that the NSV scheme effectively identifies a potential GFOV condition. Compared to the 3V0 protection scheme, the NSV scheme does not require equipment or monitoring on the high side of the substation transformer (potentially making it a lower cost alternative) and can provide faster response (since it uses precursor conditions to detect an emerging GFOV rather than waiting for actual GFOV to occur).

In the present study, a CHIL simulation approach is used to quantify the magnitude and duration of GFOV under different feeders, inverter sizes and locations, and with and without active anti-islanding.

1.4 Ground Fault Over Current

As noted in the Phase 2 Report, GFOV is not likely to arise if there is an alternate grounding source on the sub-transmission line. The alternate grounding source could be represented by a customer transformer connected electrically to the faulted sub-transmission line, as shown in Figure 3. A New York State utility indicated concern that in these situations, instead of GFOV, a prolonged ground fault overcurrent (GFOI) will be present and of such magnitude as to damage the customer transformer. The damage may ensue if the GFOI causes heating that exceeds the transformer's thermal capability.

Figure 3. Alternate Grounding Source with Variety of Winding Connections



This report examines the conditions at which GFOI may occur and determines whether there would be a need for some form of mitigation.

1.5 Objective

The objective of this research project is to develop a control-hardware-in-the-loop (CHIL) platform, comprising of the approach, methodology and software, for conducting studies of potential issues that relate to the timely and cost-effective interconnection of inverter-based PV generation in New York State distribution systems.

To demonstrate the CHIL approach, three different distribution feeders (using data provided by the specific utility) and control boards for inverter-based PV are setup to conduct simulations to better understand the following specific phenomena: (1) unintended islanding, (2) ground fault over voltage, and (3) ground fault over current.

1.6 Previous Studies

The present report presents the research and findings for what is essentially Phase 3 of a multiphase GFOV study proposed to New York State Energy Research and Development Authority (NYSERDA) by Pterra LLC.

1.6.1 Phase 1 Study

Phase 1 of the study was an initial assessment using software simulation of the nature of the GFOV phenomena. The results of Phase 1 are documented in the report titled, Assessment of Inverter-based Distributed Generation Induced Ground Fault Overvoltage on Delta-Wye Substation Transformer, Pterra Report R149-16 dated 3 January 2016 (hereinafter referred to as the "Phase 1 Study Report").[9]

The conclusions of the Phase 1 Study Report were as follows:

- GFOV is possible in the studied configuration where 2 of 3 inverter-based DG models were found able to excite the high side of transformer to high voltage. The magnitude of overvoltage depends on the ratio of DG to load on the island, performance of surge arresters when present, and the interaction of different manufacturer designs for inverter controls in the island.
- Penetration levels in terms of DG/load ratios where GFOV potential is insignificant (based on conservative assumptions and an idealized configuration).
    - Sixty-five percent—if criterion is to limit voltage to 1.38 PU
    - One hundred percent—if criterion is to avoid arrester failure, assuming arresters are the first protection against overvoltage

1.6.2 Phase 2 Study

Phase 2 of the study had the following objectives: (1) to investigate, using software simulation, the nature and characteristics of the specific form of GFOV that has certain New York State utilities requiring a 3V0 protection scheme of interconnecting DG, (b) to identify or develop an alternative protection method that may not be as onerous in cost and time penalty as the 3V0 scheme, and (c) to provide additional guidance to PV developers and utilities on how to evaluate for GFOV potential and provide future design options that will prevent or mitigate the GFOV issue. The Phase 2 objectives are met as presented in the report titled Alternate Mitigation and Design Options to 3V0 Requirement, Pterra Report R106-18, dated 2 May 2018.[10]

Using computer simulation as the basic tool, the researchers studied the behavior of various electrical parameters on the low-side of the substation transformer following inception of a single-line-to-ground fault on the high side. After trying some schemes, the researchers identified a means to detect a potential GFOV condition utilizing the low-side negative sequence voltage. The negative sequence voltage, or NSV, protection scheme was developed in this study based on the observed characteristics of sequence voltages associated with a GFOV condition.

The simulation results demonstrate that the NSV scheme effectively identifies a potential GFOV condition without inadvertent tripping. Compared to the 3V0 protection scheme, the NSV scheme does not require equipment or monitoring on the high side of the substation transformer and can provide faster response (since it uses precursor conditions to detect an emerging GFOV rather than waiting for actual GFOV to occur).

For the specific case of a 34.5-kilovolt (kV) sub-transmission system which serves several distribution substations, the researchers identified a hardware alternative to the 3V0 protection scheme. The 34.5 kV breaker located at the high-voltage substation can be replaced with a grounding breaker. This type of breaker is a combined circuit breaker and high-speed, mechanically-interlocked grounding switch. When this type of breaker trips, the attached switch grounds the line within 12 to 16 milliseconds (less than one cycle). The grounded switch then provides a ground path which eliminates the GFOV.

A 3V0 scheme, since it trips the low-side breaker of the distribution substation, only disconnects one distribution transformer from a 34.5 kV system. However, a 34.5 kV grounding breaker prevents GFOV from developing on the sub-transmission section from any of the connected distributions substations. In terms of implementation then, one installation of a 34.5 kV grounding breaker takes the role of several 3V0 protection schemes (the number depends on how many distribution substations are connected to the 34.5 kV system downstream of the grounding breaker) to prevent the same GFOV issue.

In the course of conducting the simulations to identify an alternative protection scheme, it became necessary to develop an inverter control model that represented a modern inverter with control strategies and features that can be selected and modified by the researcher (in contrast to manufacturer-provided models which are blackboxes, that is, the internal logic and functions are unknown and generally not available to modify).

To this end, the New York Purposed Inverter model was developed by the researchers in conjunction with the Manitoba HVDC Research Center. This model is compatible with the PSCAD software (developed by the Manitoba HVDC Research Center) and is available to New York State utilities for research and testing purposes. This model was used in the study as one of three inverter models included in the simulations. Before recommending a relatively expensive upgrade for the ground fault overvoltage issue, it makes sense to first review the existing system configuration to establish whether the potential GFOV issue actually exists. Key steps are as follows:

1. Check for presence of alternate grounding sources.
2. Analyze load to PV-to-load ratios.
3. Where applicable, consider the impact of surge arresters.

For future substation design and for transformer replacements at existing substations, a three-winding transformer connected Ygrounded on both the primary and secondary and delta on the tertiary is a design option that avoids the issue of GFOV.

1.6.3 Other Studies

In monitoring voltages on the low side of the substation transformer, the need for the expensive high-side PTs and a year-plus construction time may be avoided with the NSV protection scheme. However, the concept would need to be confirmed with a detailed design of the NSV implementation at either the substation or at individual PV inverters. Testing the scheme with programmed inverters or relays through a control-hardware-in-the-loop (CHIL) simulation is a possible next step to further evaluate the NSV scheme.

Finally, field tests can be conducted with devices that support the NSV protection scheme to verify if the performance matches the simulations.

1.7 This Report

This report is comprised of the following sections:

- Section 2: Simulation Setup and Models. This section describes the modeling of three feeder models provided by New York State utilities, the inverter control boards provided by manufacturers, the CHIL setup and simulation assumptions.
- Section 3: CHIL Simulation and Test. This section discusses the demonstration CHIL simulations performed, associated setup assumptions and the results with analysis and findings.
- Section 4: Conclusions

2 Simulation Setup and Models

The control-hardware-in-the-loop (CHIL) setup is comprised of the following components:

- The study feeders—data provided by New York utilities, modeled in MATLAB/Simulink[11]
- The hardware—inverter controllers provided by confidential manufacturers
- The simulation platform—OPAL-RT[12] was the software used to conduct the real-time CHIL simulations

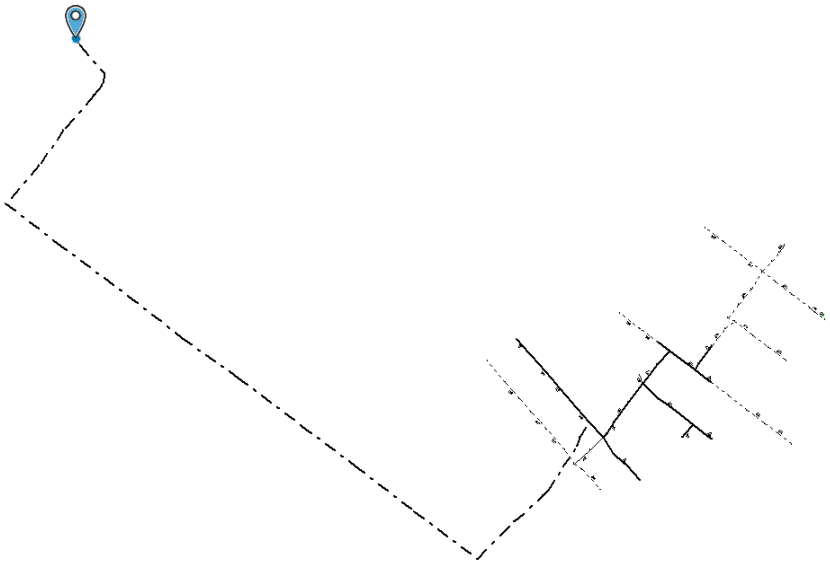
Each of the above is discussed in the following sections.

2.1 Study Feeders

Three study feeders representing New York State distribution circuits were selected for the study. Data was provided by the following New York utilities: National Grid and NYSEG.[13] The three feeder circuit models were initially provided in CYME Power Engineering Software format. These were converted to Matlab/Simulink, and then revised further to suit the real-time CHIL simulation with OPAL-RT.

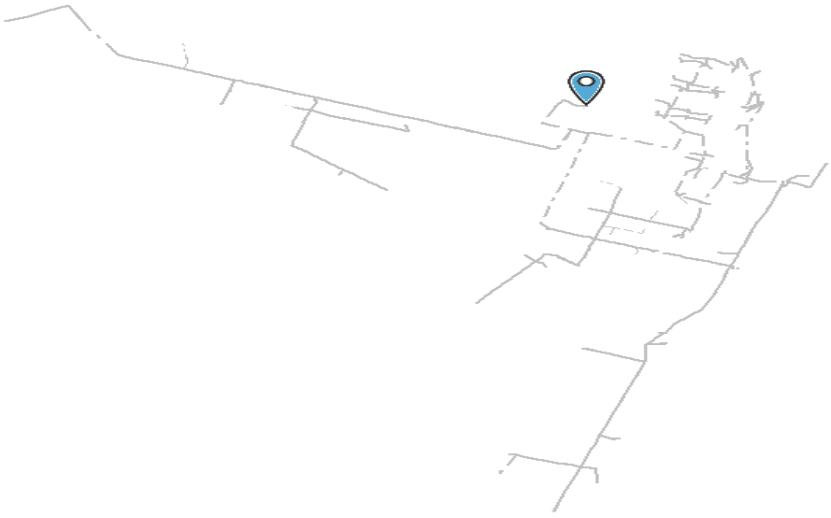
A bird's eye view of Feeder 1 is shown in Figure 4. This is a National Grid 12.47 kV feeder. The feeder has both overhead lines and underground cable as well as a single phase 100 kilovars (kVAR) capacitor bank. For demonstration purposes, the modeling of this circuit was simplified in order to fit into the capacity of the smaller of the two OPAL-RT simulators at RPI. The computer model comprised of one external source, 86 nodes, 85-line sections (of which 20 were cables and 65 were overhead lines) and six spot loads.

Figure 4. Feeder 1 Bird's Eye View



Feeder 2 is shown in Figure 5. This feeder was also provided by National Grid. The voltage level on the substation for the feeder is 13.2 kV. The feeder has both overhead lines and underground cable as well as two 900-kVAR capacitor banks. Compared to Feeder 1, Feeder 2 supports about 10 times more load, and spreads out over a larger area. Feeder 2 also features several segments branching out from the substation. The computer model is comprised of one external source, 490 nodes, 489-line sections (of which 277 are cables and 212 are overhead lines), 25 fuses, 1 recloser, 20 switches, and 75 spot loads.

Figure 5. Feeder 2 Bird's Eye View



Feeder 3 is shown in Figure 6. This feeder was provided by NYSEG and features a radial configuration with a couple of segments branching out from the substation. The voltage level on the substation for this feeder is 12.47 kV. The feeder has both overhead lines and underground cable as well as a 300-kVAR capacitor bank. The computer model is comprised of one external source, 436 nodes, 435-line sections (of which five are cables and 430 were overhead lines), one shunt capacitor, four two-winding transformers, seven switches and 167 spot loads.

Figure 6. Feeder 3 Bird's Eye View

Table 1 provides a summary of the maximum load, power factor, and grounding configuration of the three test feeders. Line-neutral loads are single phase loads typical of many residential customers.

Table 1. Summary of Total Load, Power Factor, and Configuration for the Test Feeders

Name of Feeder Circuit	Utility	Load						
		3 Phase				Line-Neutral		
		KW	KVAR	PF	Config	KW	KVAR	PF
NG_30_12867	NG	359.852	179.982	0.894	Y	334.915	168.645	0.893
NG_16456	NG	4057.013	1964.901	0.9	Y	4359.6	2111.45	0.9
NYSEG_4400701	NYSEG	1131.8	437.9	0.933	YG	802.5	614.1	0.794

2.2 Provided Inverter Controllers

Two PV inverter controllers were provided by a manufacturer[14] for CHIL simulation and testing. The basic ratings of the inverters and the input/output (I/O) requirements are shown in Table 2. Both the two inverters have the C/D design feature (C for centralized inversion and D for distributed MPPT) which optimizes the power developed from a set of PV arrays connected to the inverter. Each converter uses 15 analog input (AI) ports for receiving measuring signals from the inverter circuit and 7 digital output (DO) ports for sending out triggering signals to the inverter switching devices.

Table 2. Inverter Rating and Inverter Controllers, I/O

Inverter No.	Rated Power (kW)	Rated Voltage DC/AC (V)	Inverter Type	Required I/O for CHIL
1	500	820/315	C/D Inverter	7DO/15AI[15]
2	1000	820/520	C/D Inverter	7DO/15AI

The circuit topology of one inverter is shown in Figure 8. The main inverter components are a three-phase bridge, an inverter reactor, a filter, a contactor, and a breaker. A two-level voltage source converter is used for dc-ac conversion. The other inverter has a similar layout.

The inverters are connected at the various locations, notably near the substation, at the remote end of a feeder branch or at an intermediate point. The is intended to investigate the effect of interconnection location on the technical issues studied in this report.

Figure 7. The Diagram of PV Inverter Circuit

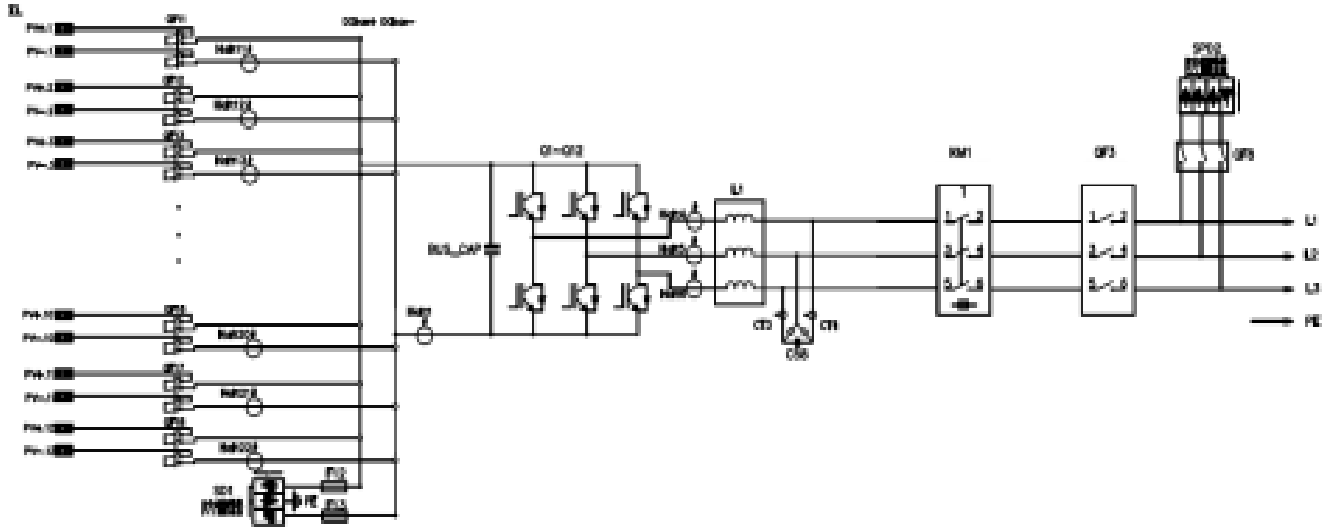
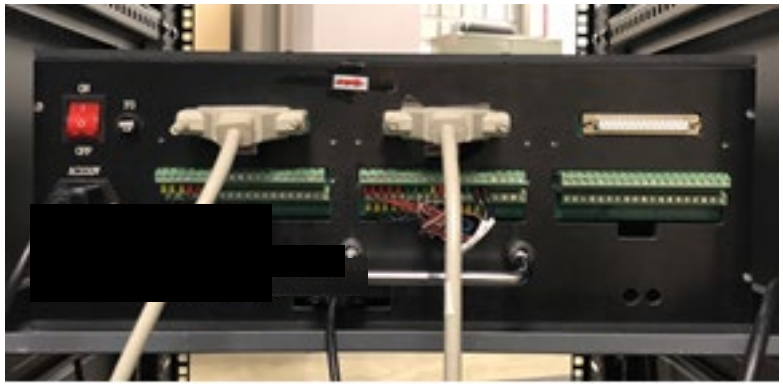


Figure 8. Overview of the PV Inverter

a) Front view



b) back view

2.3 CHIL Platform

The platform used for CHIL simulations is the OPAL-RT software. At the RPI Center for Future Energy Systems (CFES) facility, there are two real-time simulators, as follows:

- OP5600 has 12 cores (each core is an independent processing unit to allow for real-time simulation)
- Real-time SuperServer has 32 cores with a total 128 analog I/O, 208 digital I/O, 32 current and voltage measure channels for flexible controller and power Interface

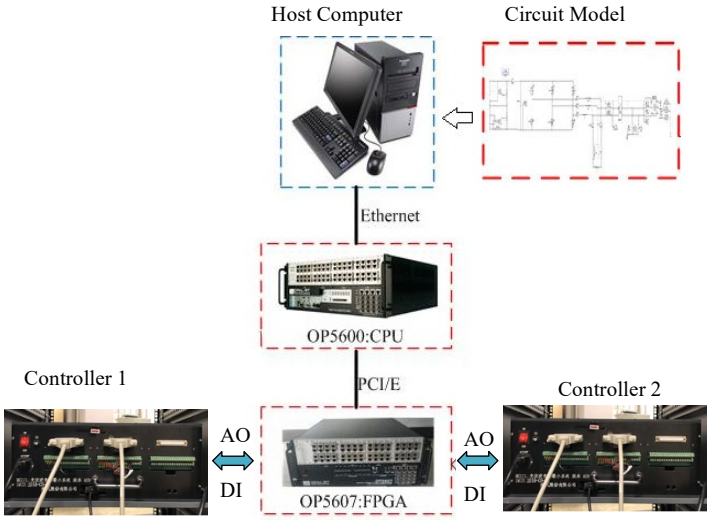
The two simulators are shown in Figure 9.

Figure 9. OPAL-RT Simulators at RPI Center for Future Energy Systems

The CHIL simulation is performed with a combination of software models and controller boards. Measuring and control signals are exchanged between the simulator, which runs the models on its cores, and the controller boards via I/O interfaces. Electrical behavior can be reproduced in real time with high fidelity.

For this study, the OP5600 simulator was used. The connection configuration is as shown in Figure 10.

Figure 10. Test Configuration for OP5600 OPAL-RT Simulators with Inverter Controllers



A host computer is used as the human-computer interface. The circuit models are built, edited, and downloaded to the simulator via the host computer. The OP5600 simulator is used for the feeder circuit simulation, with a simulation time step less than 100 µs.

The OP5607 interface box is used to interface between the simulator and the two controllers. It uses eHS technology, a generic FPGA[16]-based electrical solver provided by Opal-RT Technologies which is specifically developed for high-speed simulation of switching devices with time steps of less than 1 µs. In the study, the time step of the PV inverter circuit simulation is set at 0.5 µs. The trigger signals of the PV circuit are obtained from the hardware controllers. The analog signals such as inverter voltage and current are measured in the inverter circuit model and sent to the hardware controller thereafter.

A PCI/E optical cable is used for the fast communication between OP5600 and OP5607. An Ethernet cable is used for the slow communication between OP5600 and the host computer.

The connector setup is shown in Figure 11.

Figure 11. CHIL Setup Overview (Front View)

In order to achieve parallel-computation for fast simulation, each feeder model is partitioned using the State-Space Nodal (SSN) method. SSN is a solver using an arbitrary size for state-space that describes clusters of electrical elements and combines them into the nodal admittance matrix using the nodal method. This method virtually decouples large systems of state-space equations into smaller groups. Each of the small groups is then allocated to a core. And the speed at which each core calculates its segment of the state-space equations determines the time step of the simulation.

In order to use the OP5600 simulator, the number of nodes of the feeder model when processed with SSN must result in requiring no more than the available 12 cores.[17] To do this, some model simplifications were applied.

As an example, the model for Feeder 1 originally had 258 nodes in total, and there are around 30 cables connected in series without any components between the cables, which means the nodes can be rebuilt into equivalent blocks. Similar simplifications are applied throughout the feeder model. This reduced the number of nodes to 181. Real-time simulation of the feeder was tested using 8 cores of the OP5600 simulator at 30 μs time step. From this, it was estimated that for the largest sized feeder, Feeder 2, which has a total of 1447 nodes (490 single-line circuit nodes), a total of 27 cores are needed. Considering the simulator OP5600 only has 12 cores, the feeder-circuit models needed to be simplified further. To do so, adjacent Pi sections of overhead lines and cables without other components between them were lumped as a single Pi block, with the average unit impedance and length of the lumped Pi block calculated from the original model. In this way, the model simplification would not cause non-ignorable influences on the circuit simulation.

The required number of cores for real-time simulation in the feeders in the three studies, derived from a reduction and simplification of nodes and cores, are listed in Table 3.

Table 3. Feeder Circuits and the Required Cores for CHIL Simulation

Feeder No.	Circuit Nodes after Simplification	Required Cores for Real-Time Simulation
1	181	5
2	710	10
3	600	9

Based on the reduced feeder models, the CHIL setup, with the two controllers, at most requires 30 analog output and 14 digital input connectors for a time step of 60 μs.

2.4 Power Balance and Amplification

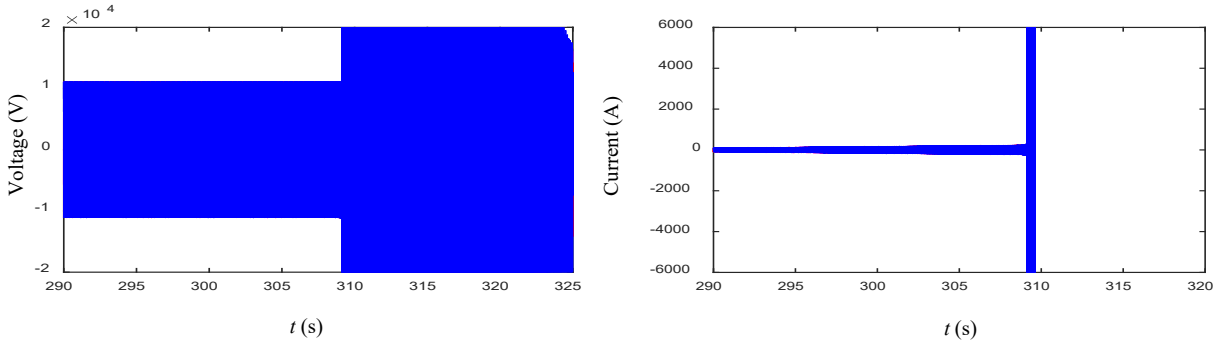
All the technical issues (islanding, GFOV, and GFOI) considered in this study require that the feeder circuit have full power balance in both real and reactive power; otherwise, the passive anti-islanding features of the inverter-based DER would trip the DER and negate any impacts related to the three issues. Full-power balance in the island will fail both tests of the Sandia Guide and require islanding mitigation per the New York Islanding Practice as described in section 1.2 of this report.

The power supply on the feeder varies from 500 to 1500 kilowatts (kW) depending on whether the 500 kW, the 1000 kW, or both inverters are connected. However, load on the study feeders varies from as low as 400 kW to as much as 4 MW (see Table 1).

In order to achieve power balance for islanding operations, a gain is added to each inverter's current output. The magnitude of the gain depends on the amount of power needed to achieve generation/load balance.

The gain, however, also amplifies harmonic currents from the inverters to a level that could lead to instability in the simulation. As shown in Figure 12, in the process of inverter startup, the inverter voltage and current outputs increase dramatically at some point of time, which indicates an unstable issue of real-time simulation. Hence, A low-pass filter and a capacitance bank are added at the interconnection point of the PV inverter to suppress the abnormal harmonics. In this case, the instability issue disappears. The capacitance bank is designed to help balance reactive power as well.

Figure 12. Inverter Voltage and Current Output in the Absence of Low-Pass Filter and Capacitance Bank



In addition to the power balance between the generation units and loads, a three-phase balance is further considered in one of the tests. (Note that the study feeders have single-phase loads connected). An additional lumped load is added to each feeder circuit with phase loads so that the circuit produces balanced currents in all three phases.

3 CHIL Simulation and Tests

This section discusses the actual test simulations conducted using the CHIL setup described in the previous section. The results of the tests are also presented and discussed, with some indicative conclusions.

Note once again, that the tests are applicable to a specific set of feeders and inverter configurations. Inverter designs and performance may vary so that any conclusions are specific to the test cases and conditions. The objective is to demonstrate a platform by which meaningful testing of inverter controllers under various circuit conditions can be conducted in a laboratory environment.

3.1 Preliminary Testing

An initial set of preliminary tests was conducted to verify the performance of the modeling assumptions and CHIL setup. Since islanding is a key condition common to all the issues being investigated, islanding tests comprised the bulk of the preliminary testing. The preliminary tests are summarized in Table 4.

Table 4. List of Preliminary Tests

Test ID	Type of Test	Balanced three-phase generation and loading power?[18]	Enabled inverter active anti-islanding function?	Inverter trip?
P-1	Islanding	Yes	Yes	Yes
P-2	Islanding	No	No	Yes
P-3	Islanding	Yes	No	No

Figure 13 presents the 1000 kW inverter output voltage, current, and power with different operating scenarios. The voltages plotted are three-phase in per unit. A detailed view of the voltage for test P-1 just before and after the inverter trips is shown in Figure 14. Here, the three phase voltages diminish to zero in less than a cycle (1/60s).

Going back to Figure 13, an inverter trip is indicated when voltage, current, and power drop to zero in the simulation. The inverter trip is indicated in tests P-1 and P-2 (see plot of Power). In test P-3, the power does not reduce to zero indicating that the inverter does not trip.

Figure 13. Inverter Islanding Operation under Different Conditions

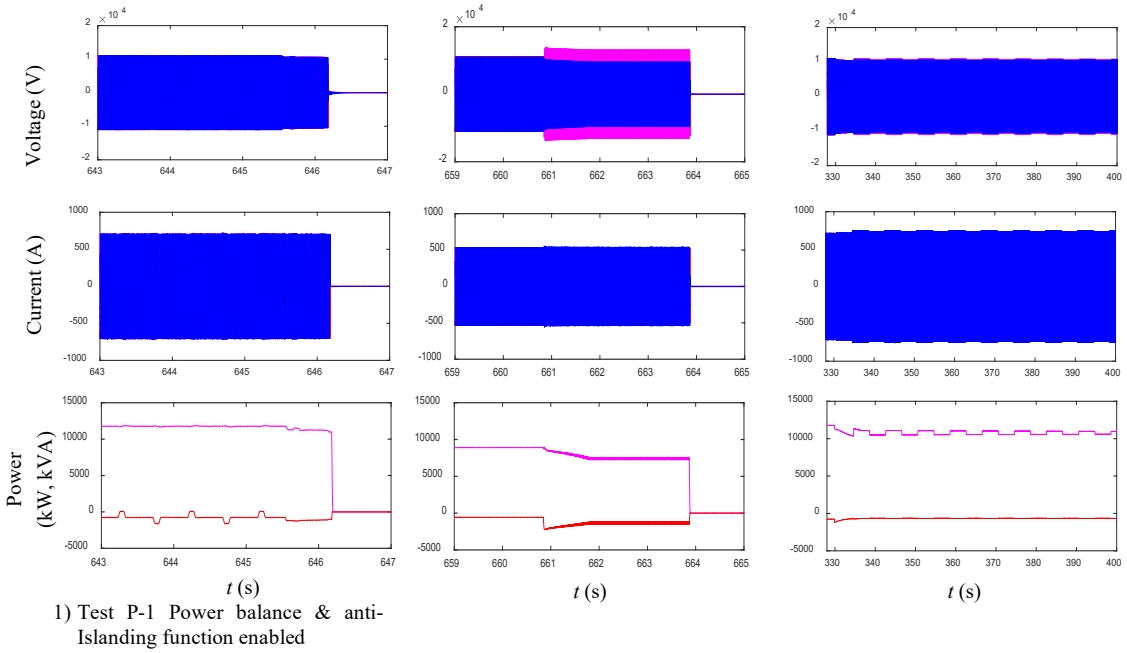
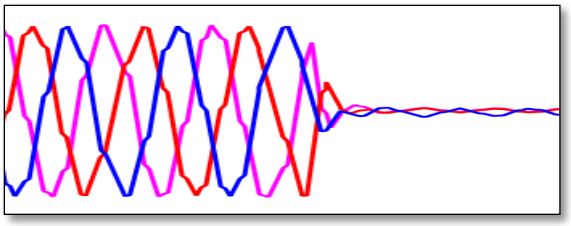


Figure 14. Detailed View of Voltage in Test P-1 before and after the 1000-Kilowatt Inverter Trips



From these preliminary tests, it is noted that the active anti-islanding feature of the specific inverters used in the CHIL simulations will trip the inverter under both imbalanced and fully balanced[19] conditions. It is further expected that if the island is unbalanced, the inverter will trip on its passive anti-islanding protection even if the active anti-islanding is disabled.

3.2 Time-Step Setting for Real-Time Simulation

This section discusses the selection of time step that enables the real-time simulations used in the study. The CHIL simulation setup using OPAL-RT allows for real-time simulation. Recording of simulation parameters such as voltage, current, and power is made after each simulation time step. However, the

time-step size will depend on the processing speed of the individual processors in the setup as well as the transmission and switching times between and among the software and hardware components. For this particular study, the simulation time step is determined by the following factors:

- the switching frequencies of the PV inverters and feeder simulation
- transmission time between the OPAL-RT's OP5600 simulator and the hardware controllers
- the transient behavior of the Single Line-to-Ground Fault (SLGF) for the GFOV study

The following discussion addresses the individual CHIL setup components to determine the minimum time step each will be able to provide. The largest of these values determines the time step used for the simulations.

1. Inverter circuits. The PV inverter circuits are modeled in the OP5607 device. This box is based on FPGA technology and is capable of conducting real-time simulation with a time step less than 0.5 μs for a circuit with a total of 128 switching devices.
2. Feeder circuits. The feeder circuits, on the other hand, are modeled in the OP5600 box, which contains 12 cores or independent processing units. Each feeder model is partitioned using the State-Space Nodal (SSN) method.20 After partitioning, basic tests indicate that the minimum time step for the slowest feeder to simulate is 60 μs.
3. Communications. Taking into account the required input and output signals and the communication function between OP5607 and the hardware controllers, the minimum time step for the study's CHIL simulation increases to 80 μs.
4. In the following discussion, time constants of the SLGF are calculated to identify the required time step for fault transient simulations.

The high-voltage side circuit of the substation transformer is represented by a three-phase voltage source block with L-R branches in series. Taking Feeder 2 as an example, the system inductance and resistance are calculated as follows:

Equation 1

$$L_s = \frac{V_{base}{}^2}{2\pi f_n P_{sc}} = \frac{13200^2}{2\pi \times 60 \times 594 \times 10^6} = 0.7781\text{mH}$$

Equation 2

$$R_s = \frac{2\pi f_n L_s}{K_{X/R}} = \frac{0.2933}{20.63} = 0.0142\Omega$$

Thus, the lowest time constant of the SLGF is obtained as

$$\tau_s = \frac{L_s}{R_s} = \frac{0.7781 \times 10^{-3}}{0.0142} = 0.0548$$

Equation 3

1. A typical rule-of-thumb for accurate simulation is to set the time step to be less than 10% of the time constant, or, in this case, about 5 milliseconds (ms) or 5000 μs. Since it has already been determined that the CHIL setup for this study will allow an 80 μs time step, then the simulation should be able to capture the SLGF event accurately.
2. The oscillation frequency of the feeder circuits may also present a limiting condition for selecting the simulation time step. The following discussion presents the derivation of the oscillation frequency.
   For the circuit behind the transformer, the root-mean-square (RMS) of transformer distributed side voltage and current are measured as 5887 V and 7433 A, respectively. The positive-sequence voltage and current are measured at $8730/\sqrt{2}$ and $11265/\sqrt{2}$, respectively. The reactive power of a single-phase capacitance bank is 300 kVA, with nominal RMS voltage 7621V. Then the lumped capacitance is calculated as:

$$C = \frac{Q_c}{V_{RMS}{}^2 \omega} = \frac{600 \times 10^3}{7621^2 \times 377} = 27.4\mu\text{F}$$

Equation 4

The current of the lumped capacitance bank is obtained by

$$\dot{I}_C = \frac{8730\angle 16}{\sqrt{2}} \times 377 \times 27.4 \times 10^{-6} \angle 90 = 63.77\angle 106$$

Equation 5

The current of the lumped load and the lumped load impedance are calculated as

$$\dot{I}_{LD} = \frac{11265\angle -20}{\sqrt{2}} - 63.77\angle 106 = 7502.8 - j2785.7 \approx 8003\angle -20.4$$

Equation 6

$$Z_{LD} = \frac{8730\angle 16}{\sqrt{2}} / 8003\angle -20.4 = 0.77\angle 36.4$$

Equation 7

Thus, lumped resistance and inductance of the series RL load are

Equation 8

$$\begin{cases} R_{LD} = 0.77\cos(36.4) = 0.62\Omega \\ L_{LD} = \dfrac{0.77\sin(36.4)}{2\pi f_n} = \dfrac{0.46}{2\pi f_n}\Omega = 1.22\text{mH} \end{cases}$$

Similarly, the lumped resistance and inductance of the parallel RL load are calculated as

Equation 9

$$\frac{8730}{\sqrt{2}R_{LD}} + \frac{8730}{j\sqrt{2}\times 377\times L_{LD}} = 8003\angle -36.4$$

Equation10

$$\begin{cases} R_{LD} = 0.96\Omega \\ L_{LD} = 3.44\text{mH} \end{cases}$$

Thus

Equation 11

$$C_{LD} = L_{LD}\left(\frac{Q}{R_{LD}}\right)^2,\ \tau_L = R_{LD}C_{LD} = \frac{L_{LD}\cdot Q^2}{R_{LD}} = 3.58\times 10^{-3}Q^2$$

Equation12

$$\omega_L = \frac{1}{\sqrt{L_{LD}C_{LD}}}\sqrt{1-\frac{C_{LD}{R_{LD}}^2}{L_{LD}}} \le \frac{1}{\sqrt{L_{LD}C_{LD}}} = \frac{R_{LD}}{L_{LD}Q} = \frac{279}{Q},\ f_L = \frac{44.4}{Q}$$

The quality factor of the circuit will be larger than 0.5, and the potential oscillation frequency of the RLC load will be less than 90 Hz. Again, an applicable rule-of-thumb for simulation of oscillatory phenomena is to have a time step of 10% of the duration of one cycle. In this case, that time step is 11 ms (11,000 µs).

The study time step of 80 µs is also sufficient to simulate the circuit oscillation.

3.3 CHIL Simulation and Testing

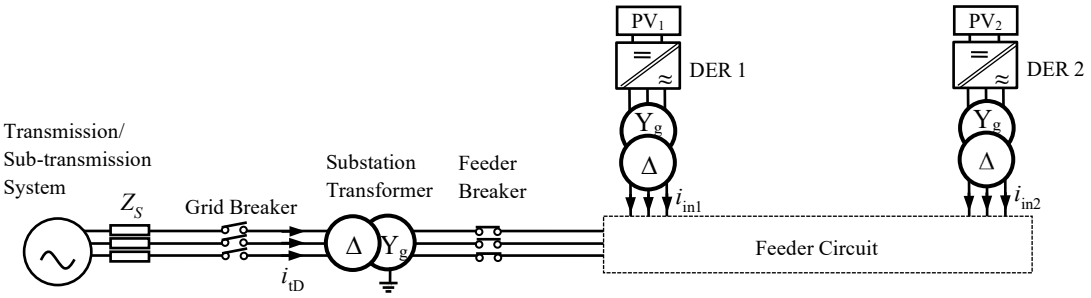
A set of CHIL simulations were conducted to test the characteristics of the two study inverters with respect to operation on the three study distribution feeders under three different technical issues that may impact interconnection of DER. The following subsections discuss tests for each of the following:

- Unintended islanding
- Ground fault overvoltage (Two types: SLGF on the subtransmission line and on the distribution feeder)
- Ground fault overcurrent

3.3.1 Unintended Islanding

The generic circuit diagram for the islanding tests is shown in Figure 15. The feeder circuit can be any of the three feeders described in Section 122.1. The location of the inverter(s) can likewise vary. The test is initiated when the grid breaker is opened.

Figure 15. Circuit Diagram of Islanding Study



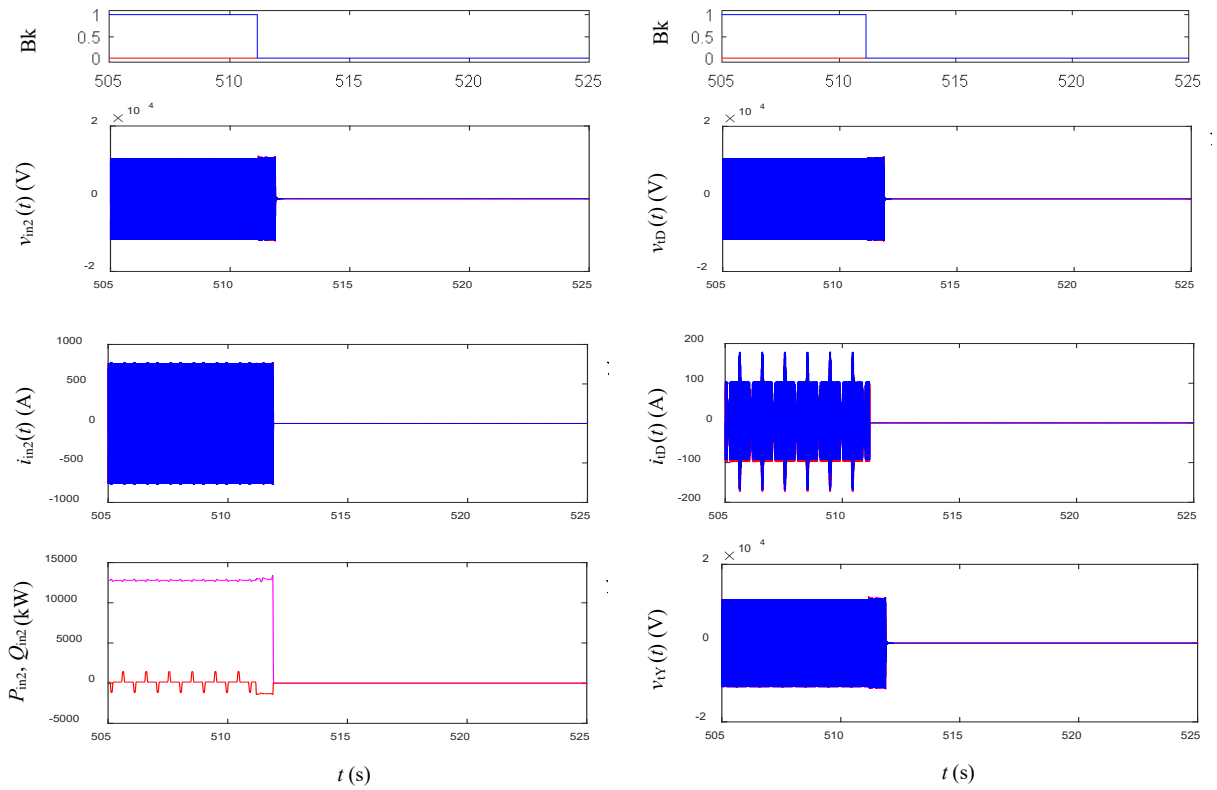
The typical response of islanding operation with the inverter active anti-islanding function enabled is demonstrated in Figure 16.

- $v_{in2}(t)$ and $i_{in2}(t)$ are the Inverter 2[21] output voltage and current, respectively
- P_{in2}, and Q_{in2} are the Inverter 2 real and reactive power output respectively
- $v_{tD}(t)$ and $i_{tD}(t)$ are substation transformer voltage and current on delta side, respectively,
- $v_{tY}(t)$ is the substation transformer voltage on wye side
- Bk is the triggering signal for grid breaker (blue) and fault breaker (red); where a value of 1 indicates the breaker is closed, and a zero means the breaker is open

The x-axis shows the clock time of the simulator in seconds. The grid breaker is opened at t=511.2s clock time. The opening of the breaker results in the feeder being islanded with the inverters online. Active anti-islanding protection shuts down the inverter about 0.7s later. Note the pulses in Q_{in2} and $i_{in2}(t)$. These are presumed to be the reactive power pulses injected by the study inverter as part of its active anti-islanding feature. (Other inverter designs may use other methods for active anti-islanding detection.) The pulses are about 0.5s apart alternating between positive and negative quantities.

Figure 17 shows the response to an islanding event when inverter active anti-islanding is disabled. Here, the grid breaker is switched off at t=720.5s. The inverter does not trip and continues to power the islanded feeder.

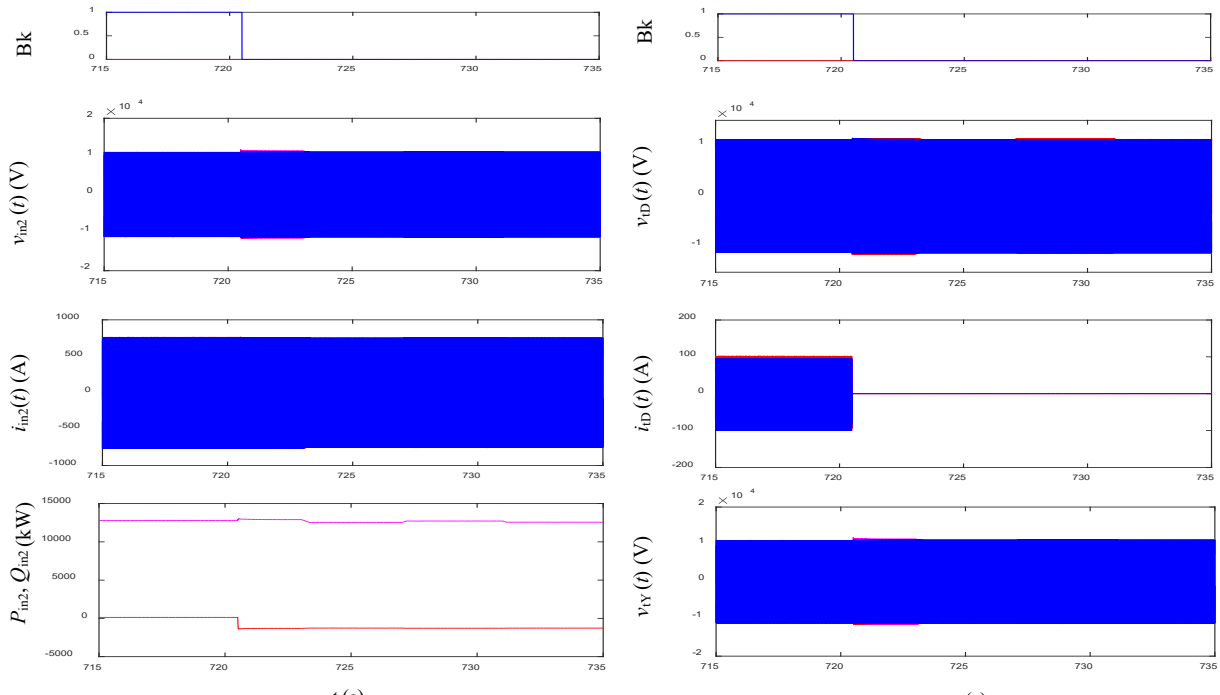
Figure 16. Inverter Islanding Operation with Active Anti-Islanding Function Enabled



1) Inverter output

2) Substation transformer voltage & current

Figure 17. Inverter Islanding Operation with Anti-Islanding Function Disabled



1) Inverter output

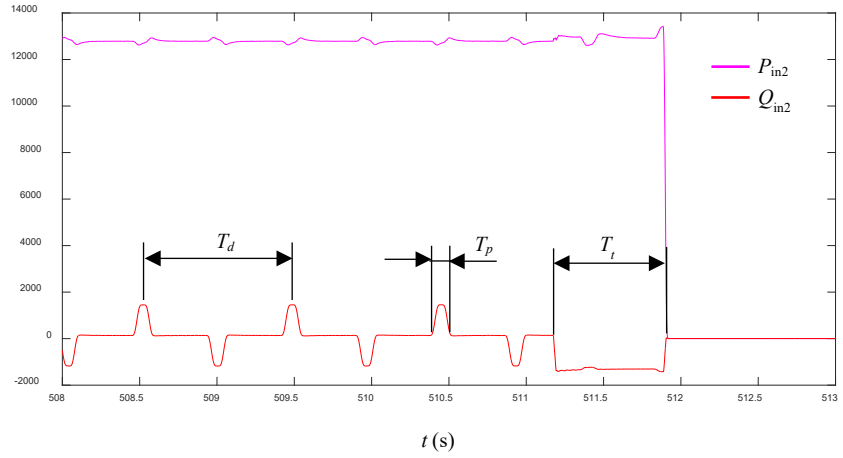
2) Substation transformer voltage & current

Figure 18 shows a close-up look at the effect of the active anti-islanding pulses on the real and reactive power output from Inverter 2. The pulses are more pronounced in the reactive power output. They have a steady duration and period with characteristics as follows:

- Pulse width, T_p, is 0.13s
- Pulse period, T_d, is 0.965s

The pulses alternate between positive and negative values. The time between the end of the previous pulse to the start of the next pulse is 0.353s. When the fault is initiated, the regular pulse is interrupted, and shortly thereafter, the inverter trips. The time from the when the feeder breaker opens to when the inverter trips is designated as T_t.

Figure 18. Close-Up View of Inverter Pulses as Seen in the Real and Reactive Power Output



To investigate the distribution of inverter tripping time, the following two test cases were considered:

- Test S-1: Islanding detection test with single inverter connected to Feeder 1.
- Test S-2: Islanding detection test with two inverters connected to Feeder 1.

In both test cases, the active anti-islanding feature of the inverters were activated. Both tests were repeated several times with the circuit and inverter operating conditions unchanged. The timing of the feeder breaker trip to initiate islanding was selected randomly.

The statistics of the inverter trip time for the two Test Cases, S-1 and S-2, are summarized in Table 5. For Test Case S-1, with only one inverter in the study feeder, the mean for T_t is 0.779s, with a standard deviation of 0.219s. The 90th and 99th percentile values[22] are 1.059s and 1.288s. These are within the 2-second limit for tripping time specified in IEEE Standard-1547. (Note that given the pulse period of

0.965s, and that there are two pulses, one positive and the other negative, within this period, the response time of the inverter is within two to three pulses from the initiation of the islanding event. Apparently, the inverter will not trip on the first abnormal pulse response but waits for at least a second pulse to confirm the islanding condition.)

Table 5. Statistics of Inverter Tripping Time T_t for Test Cases S-1 and S-2

Case & Inverter[23]	Minimum Value	Maximum Value	Mean	Standard Deviation	90th percentile	99th percentile
Inverter 1 in case S-1	0.499	1.125	0.779	0.219	1.059	1.288
Inverter 1 in case S-2	0.569	1.233	0.879	0.230	1.175	1.415
Inverter 2 in case S-2	0.578	1.056	0.795	0.134	0.966	1.105
Both Inverters in case S-2	0.578	1.233	0.888	0.227	1.179	1.415

For Test Case S-2, there are two inverters. Both inverters use the same anti-islanding method with the same values for pulse width and period. However, their pulses are not simultaneous with each other, and the difference between positive pulses from Inverters 1 and 2 is random. In the sampling tests, the two inverters change places as to which one would trip first. Inverter 2 has the lower mean for trip time at 0.795s compared to 0.879s for Inverter 1. (Both values for mean are larger than the solo inverter in Test Case S-2. *There is apparently some delay in trip time introduced by having two inverters on the feeder compared to having just one.*) The standard deviation for Inverter 1 is 0.230s which is very similar to its standard deviation under Test Case S-1 where it is the only inverter on the feeder. In comparison, the standard deviation for Inverter 2 is 0.134s. This is much smaller than the standard deviation of Inverter 1 implying that although the two inverters have similar methods for active anti-islanding detection with the same pulse width and period, their response times to an islanding event are dissimilar. The time to trip both inverters in Test Case S-2 is slightly longer than the single inverter in Test Case S-1, with mean time of 0.888s and 99th percentile of 1.415s, compared to 0.779s and 1.288s, respectively. This also supports the previous observation that there is an apparent delay in trip time when two inverters are on the feeder, but the delay is no more than the time to an extra pulse. It is also observed that once the first inverter trips, the remaining inverter trips not only on its own active anti-islanding protection but may also trip on its passive anti-islanding function, since the feeder conditions will now show unbalanced voltage and frequency.

The inverter trip time is a function of when the islanding occurs in relation to the point in time within the inverter pulse period. If an islanding event occurs immediately after a detection pulse, the inverter takes just a little more time to detect the island compared to an event which occurs just before a pulse.

Furthermore, the interaction effect of multiple-inverter applications is determined by the detection technologies used by the inverters. Exhaustive experiments with various inverters employing various detection technologies and related analysis are needed to obtain a general conclusion of the interaction in multiple inverter environments. This is beyond the scope of this study which is intended to demonstrate the platform and methodology for conducting such experiments and testing.

The summary of the tests and results for islanding is shown in Table 6.

Table 6. Summary of Islanding Tests

Test ID	Active Anti-Islanding Enabled?	Location of Inverter[24]		Feeder	Trip Time[25]	
		1000 kW	500 kW		1000 kW Inverter	500 kW Inverter
1-1	No	A		1	Did not trip	
1-2	No	D		1	Did not trip	
1-3	No		A	1		Did not trip
1-4	No		D	1		Did not trip
1-5	No	A	D	1	Did not trip	Did not trip
1-6	No	D	A	1	Did not trip	Did not trip
1-7	No	B	C	1	Did not trip	Did not trip
1-8	Yes	A		1	Within 2-3 pulses	
1-9	Yes	D		1	Within 1-2 pulses	
1-10	Yes		A	1		Within 2-3 pulses
1-11[26]	Yes		D	1		Within 2-3 pulses
1-12	Yes	A	D	1	Within 2-3 pulses	Within 3-4 pulses
1-13[27]	Yes	D	A	1	Within 1-2 pulses	Within 1-2 pulses
2-1	No	A	D	2	Did not trip	Did not trip
2-2	No	D	A	2	Did not trip	Did not trip
2-3	Yes	A	D	2	Within 1-2 pulses	Within 3-4 pulses
2-4	Yes	D	A	2	Within 1-2 pulses	Within 2-3 pulses
3-1	No	A	D	3	Did not trip	Did not trip
3-2	No	D	A	3	Did not trip	Did not trip
3-3	Yes	A	D	3	Within 2-3 pulses	Within 2-3 pulses
3-4	Yes	D	A	3	Within 1-2 pulses	Within 2-3 pulses

When active anti-islanding is disabled, the inverters fail to trip within 2 seconds. Remedial measures, such as direct-transfer trip (DTT), are needed for this situation. The DTT should initiate on the opening of the feeder breaker and send a trip signal to cause tripping of the inverter(s) within six to12 cycles (0.1 to 0.2 seconds).

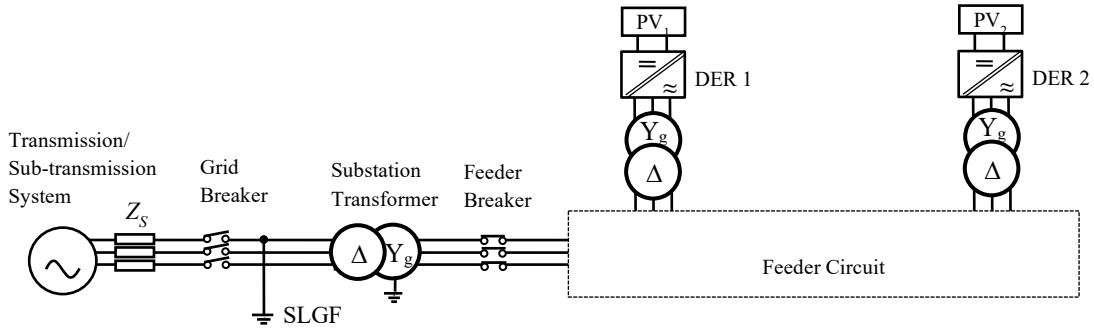
When the study inverters' active anti-islanding protection is enabled, the 1000 kW inverter tends to trip within one to three pulses[28] regardless of feeder type, location in the feeder, or whether or not another inverter is on the feeder. The 500-kW inverter has a slower response requiring at least two pulses and, in two highlighted test cases (one to12 and two to three), up to four pulses (between 1.448s and 1.93s). Both inverters comply with the 2s limit on response time specified in IEEE Std-1547.

The slower trip times for an inverter apply to specific system conditions including (a) presence of another inverter on the circuit, (b) the inverter is located on the remote end from the feeder breaker, and (c) the inverter is on a feeder with no capacitor bank.

3.3.2 Ground Fault Overvoltage on the Subtransmission Line

The generic circuit diagram for the ground fault overvoltage (GFOV) on the subtransmission line test is shown in Figure 19. This is similar to the generic circuit for islanding (see Figure 15) with the addition of a solid single line-to-ground fault (SLGF) on the high side of the substation transformer. The test is initiated with the SLGF applied to phase A. The grid breaker opens five cycles later, where the five cycles allow time to detect the fault and the breaker to open.

Figure 19. Circuit Diagram for GFOV Study



The typical response for the GFOV test with inverter anti-islanding function enabled is presented in Figure 20.

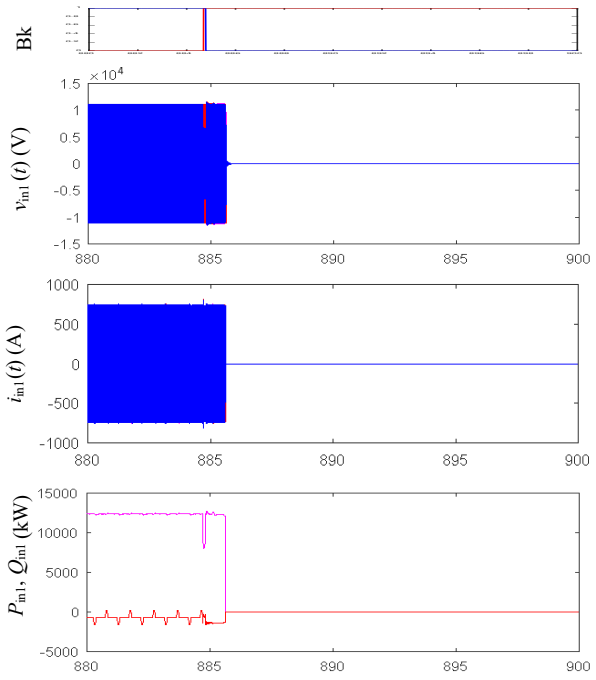
- $v_{in1}(t)$ and $i_{in1}(t)$ are the Inverter 1[29] output voltage and current, respectively
- P_{in1}, and Q_{in1} are the Inverter 1 real and reactive power output respectively
- $v_{tD}(t)$ and $i_{tD}(t)$ are substation transformer voltage and current on delta side, respectively
- $v_{tY}(t)$ is the substation transformer voltage on wye side
- Bk is the triggering signal of grid breaker (blue) and fault breaker (red)

As shown, the SLGF is initiated at t=884.7s. Five cycles later, the grid breaker is opened isolating the faulted island. GFOV initiates at 1.732 times the pre-fault voltage on phases B and C on the delta side of the substation transformer. The inverter begins shutting down at about t=885.6s.

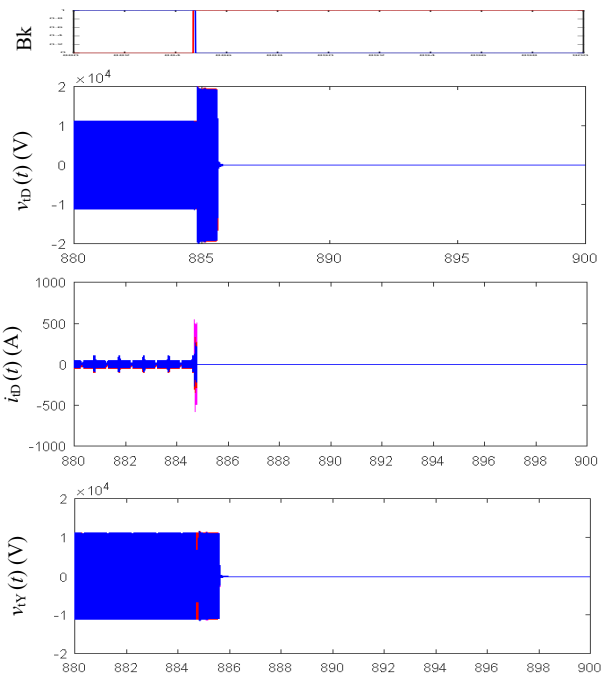
The response for the GFOV test with inverter anti-islanding function disabled is presented in Figure 21. In this case, the fault is applied at t=679.6s. After five cycles, the grid breaker opens. The inverter continues to energize voltages of phase B and C on the delta side of the transformer at 1.732 times the pre-fault voltage.

Note that in both cases shown in Figure 20 and Figure 21, the low voltage ride through (LVRT) capability of the inverter is enabled.

Figure 20. 3V0 Test with Inverter Anti-Islanding Function Enabled

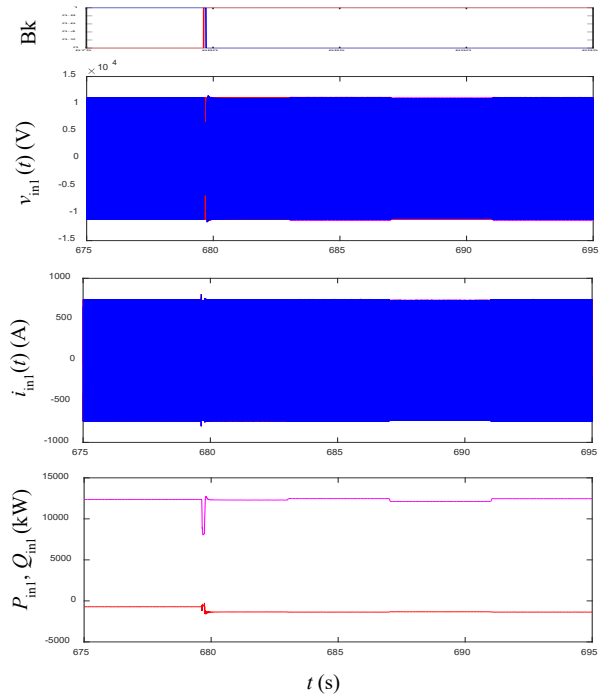


1) Inverter output

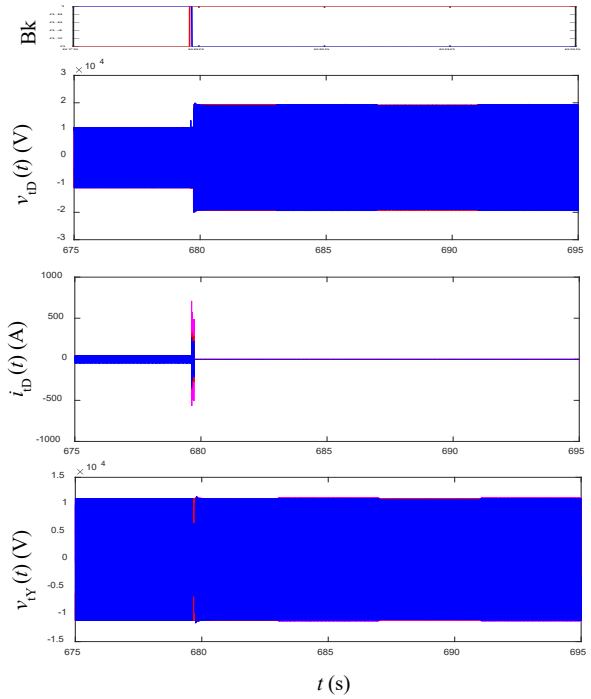


2) Substation transformer voltage & current

Figure 21. 3V0 with Inverter Anti-Islanding Function Disabled



1) Inverter output



2) Substation transformer voltage & current

The summary of the tests and results for GFOV is shown in Table 7.

Table 7. Summary of Tests and Results for Ground Fault Overvoltage

Test ID	Feeder	Active Anti-Islanding Enabled?	Location of Inverter30		Trip Time31		Overvoltage Magnitude (PU)	
			1000 kW	500 kW	1000 kW Inverter	500 kW Inverter	Delta Side of Transformer	Y Side of Transformer
1-14	1	No	A		Did not trip		1.73	1.03
1-15		No	D		Did not trip		1.73	1.03
1-16		No		A		Did not trip	1.73	1.03
1-17		No		D		Did not trip	1.73	1.03
1-18		No	A	D	Did not trip	Did not trip	1.73	1.03
1-19		No	D	A	Did not trip	Did not trip	1.73	1.03
1-20		No	B	C	Did not trip	Did not trip	1.73	1.03
1-21		Yes	A		Within 1-2 pulses		1.73	1.03
1-22		Yes	D		Within 1-2 pulses		1.73	1.02
1-23		Yes		A		Within 1-2 pulses	1.73	1.01
1-24		Yes		D		Within 1-2 pulses	1.73	0.98
1-25		Yes	A	D	Within 1-2 pulses	Within 1-2 pulses	1.73	1.01
1-26		Yes	D	A	Within 1-2 pulses	Within 1-2 pulses	1.73	1
1-27		Yes	B	C	Within 1-2 pulses	Within 3-4 pulses	1.73	1
2-5	2	No	A	D	Did not trip	Did not trip	1.75	1.02
2-6		No	D	A	Did not trip	Did not trip	1.75	1.02
2-7		Yes	A	D	Within 1-2 pulses	Within 2-3 pulses	1.75	1.02
2-8		Yes	D	A	Within 2-3 pulses	Within 3-4 pulses	1.75	1.02
3-5	3	No	A	D	Did not trip	Did not trip	1.73	1.03
3-6		No	D	A	Did not trip	Did not trip	1.73	1.03
3-7		Yes	A	D	Within 1-2 pulses	Within 1-2 pulses	1.73	0.975
3-8		Yes	D	A	Within 1-2 pulses	Within 1-2 pulses	1.73	0.975

Following a GFOV event, voltages as high 1.75 per unit are observed (in tests 2-6 through 2-10) on the high side of the substation transformer. These results are consistent with the software simulation (from the Phase 2 Study).

When active anti-islanding is disabled, the inverters fail to trip. With active anti-islanding, the range of response is from within one pulse to as long as four pulses. Although, this is within the 2s islanding response time, the duration of the overvoltage may be too long for equiment and personnel. Remedial measures, such as 3V0 and the negative-sequence voltage (NSV)[32] protection schemes, are needed for this situation.

3V0 protection will wait until the sensing relay detects the overvoltage and sends a trip signal to the feeder breakers. This could take as long as 6–24 cycles (0.1 to 0.4 seconds) to occur, just a little bit faster than active anti-islanding protection. In the meantime, the overvoltage remains on the high voltage side.

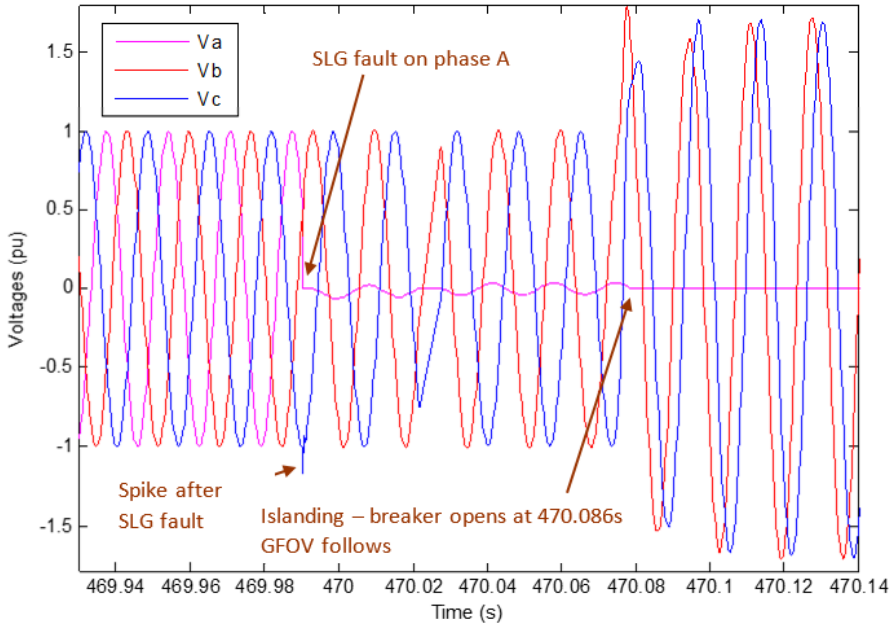
The proposed NSV scheme will detect the overvoltage as soon as it occurs and trigger the inverter to trip faster than the 3V0 scheme, within one to two cycles. This is a faster and preferred response considering that the overvoltage is a safety risk. The following discussion notes the characteristics of the system response that supports the implementation of the NSV scheme. A more detailed description of the NSV scheme is included in the report prepared for NYSERDA titled Alternate Mitigation and Design Options to 3V0 Requirement, Pterra Report R106-18, dated 2 May 2018.

First, we take a closer look at a representative response to the SLGF that initiates the GFOV event. Figure 22 shows phase voltages for Test Case 1-21 (Feeder 1 with the 1000 kW inverter located near the feeder breaker. Active anti-islanding is enabled.) In Figure 22(a), it can be observed that as the SLGF is applied to phase A, the phase B and C voltages continue at their pre-fault levels until the utility breaker opens five cycles later. After the utility breaker opens, the phase B and C voltages rise to 1.732 times the pre-fault magnitude. Not shown in the figure is the extinguishing of the high side voltages as the 1000 kW inverter trips. The inverter trips after its active anti-islanding protection detects the island formed by the opening of the utility breaker. As noted earlier in this report (see section 3.3.1), the time within which the inverter protection responds will vary depending on when the island forms relative to its pulse cycle. In this particular case, the inverter trips within one to two pulses after the island is formed which, based on the pulse duration of the inverter, is no more than 0.965s. This is a fast response, but the brief period of over voltage may still impact equipment and pose a safety risk.

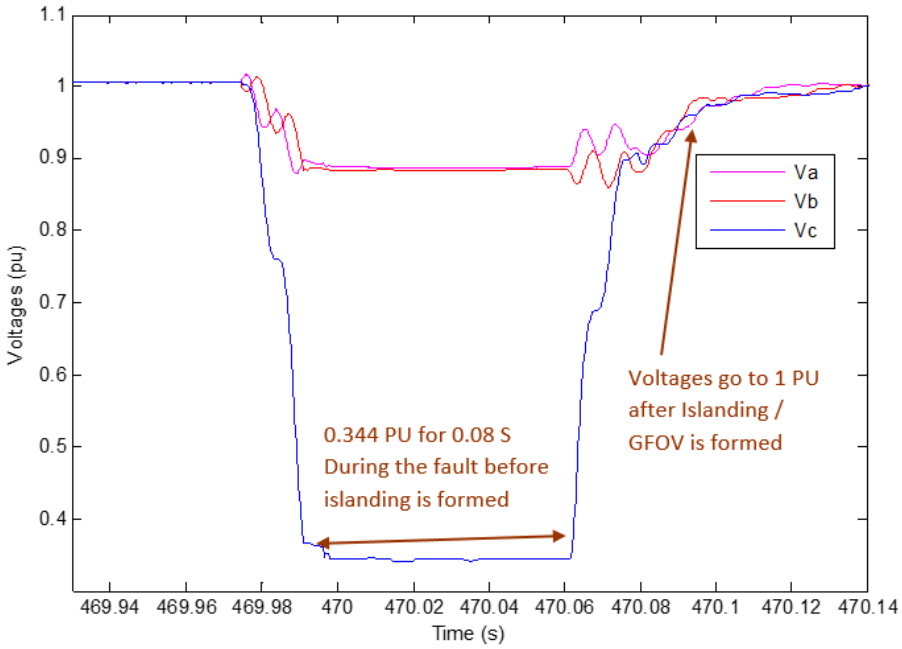
Figure 22 (b) plots the RMS value of phase voltages at the terminals of the 1000 kW inverter. The inverter is initially operating at lagging power factor. When the SLGF is applied, the phase voltages at the inverter terminal start to drop. The phase C voltage[33] drops to 0.35 PU for about 0.08s. Since the LVRT feature is enabled, the inverter does not trip on low voltage of this short duration. After the utility breaker opens, the inverter voltages gradually recover to the pre-fault level. The voltages will remain in this state until the inverter trips on its active anti-islanding protection.

Figure 22. Case 1-21 Voltage Waveform Plots Showing Events with the SLG Fault and Islanding/Utility Breaker Open

(a) High Side Voltages



(b) RMS Voltages at Terminal of Inverter 2

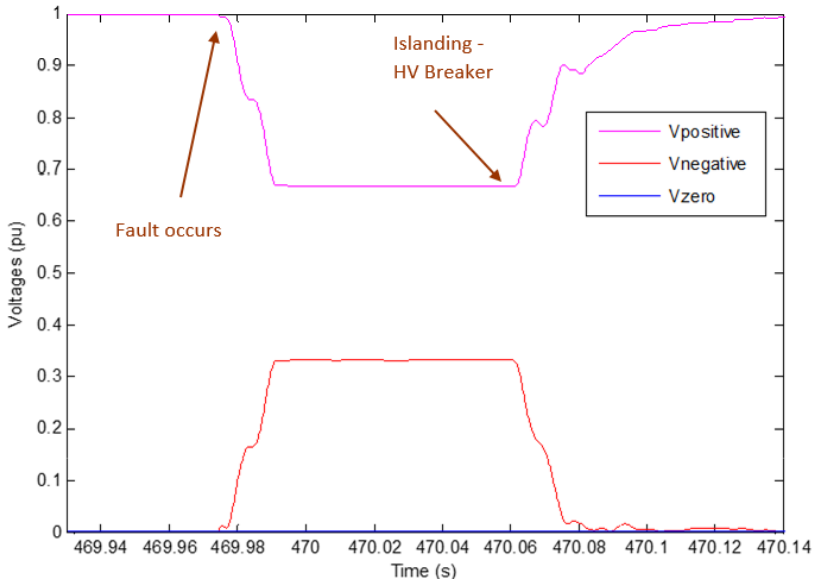


For the NSV protection scheme, the response is based on the sequence voltages. Figure 23 shows the symmetrical voltage waveform plots for the same test case. Following application of the SLGF, the high-side positive sequence voltage drops, while the negative sequence voltage rises [Figure 23(a)]. Within a cycle, both the positive and negative sequence voltages reach their target values and stay there until the utility breaker opens. After the breaker opens, the sequence voltages recover to their pre-fault level. The magnitude of incremental change is almost identical in the negative and positive sequence voltage [Figure 23(b)]. This response is consistent with simulations discussed in the Phase 2 Report, and thus confirms that the NSV protection scheme will be able to detect the incipient GFOV condition and trip the inverter at a much faster response than the 3V0 scheme.

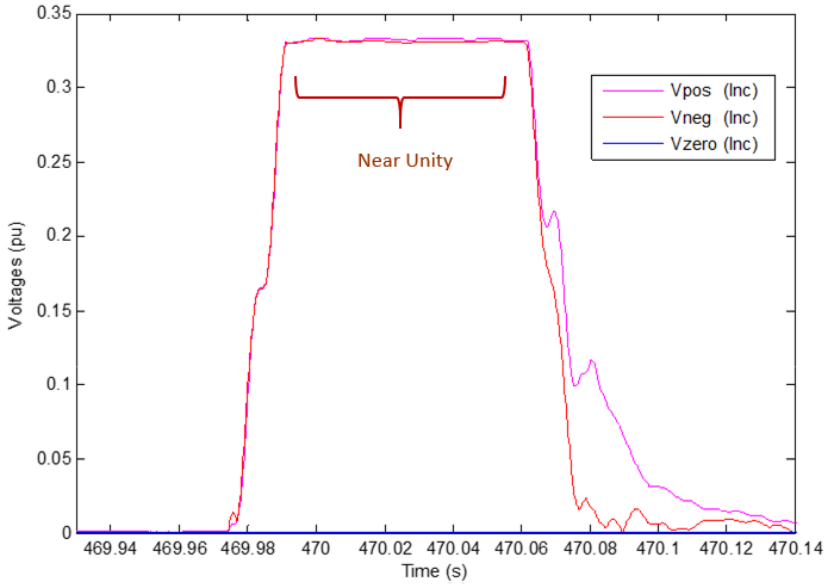
For the specific inverters tested here, the inverter trip occurs due to the anti-islanding protection, which as noted previously depends on a 0.965 cycling period for its detection signal. These particular inverters do not detect the overvoltage, unlike some simulation models that were studied for the Phase 2 Report. Other types and designs of inverters may be able to trip faster by detecting the overvoltage event or by using shorter anti-islanding detection cycles.

Figure 23. Case 1-21 Symmetrical Voltage Waveform on the Inverter Side

(a) Inverter Voltage



(b) Incremental Voltage



3.3.3 Ground Fault Overvoltage on the Distribution Voltage

Ground fault overvoltage may also occur on the distribution voltage. A SLGF fault anywhere on the feeder will cause the feeder breaker to open, islanding the feeder with its connected DER.

Table 8 shows a summary of two tests conducted for GFOV on Feeder 2 with two inverters connected. The configuration is as shown in Figure 19, but with the SLGF applied at the terminal of the 1000 kW inverter. For conservatism, the low voltage ride-thru function is enabled for both inverters (otherwise, the inverters may trip when voltage drops following the fault). Furthermore, active anti-islanding protection is disabled. This is to determine the duration of any GFOV without action from active anti-islanding.

For test 2-9, the load and generation on the island is balanced. The plots of test results are shown in Figure 24.

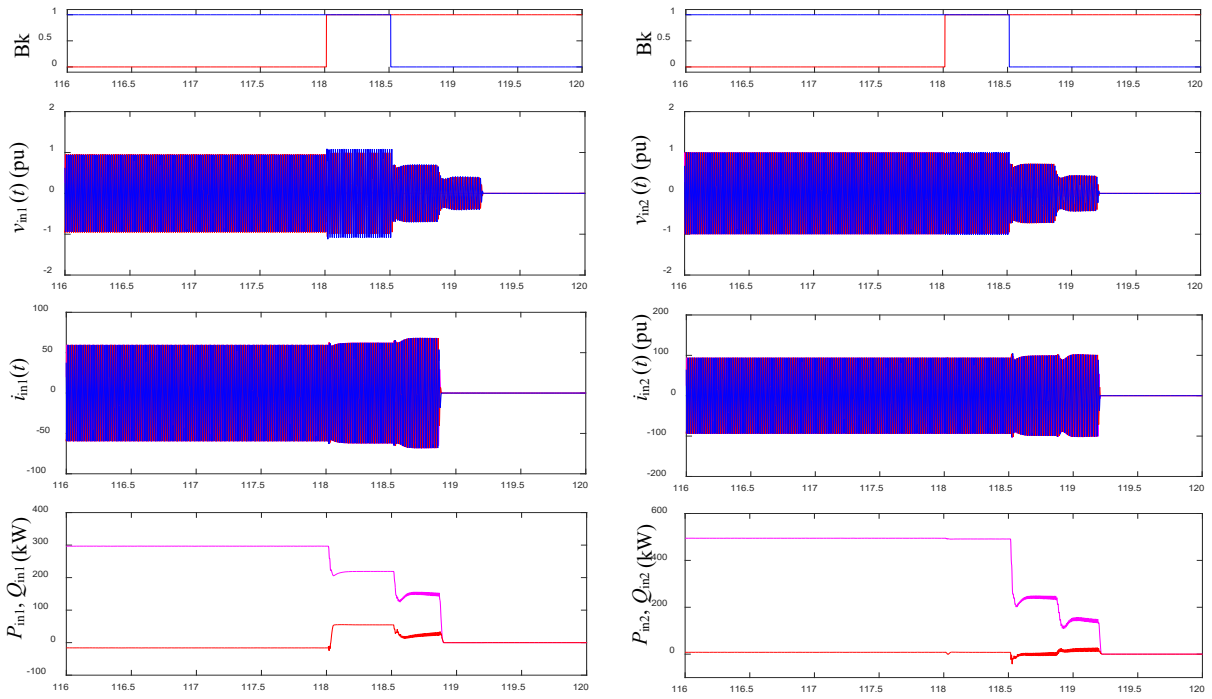
- Bk is the triggering signal of feeder breaker (blue) and fault breaker (red)
- $v_{in1}(t)$ and $v_{in2}(t)$ are the Inverter 1 and 2^{34} output voltages, respectively
- $i_{in1}(t)$ and $i_{in2}(t)$ are the Inverter 1 and 2 output currents, respectively
- P_{in1}, and Q_{in1} are the Inverter 1 real and reactive power output respectively
- P_{in2}, and Q_{in2} are the Inverter 2 real and reactive power output respectively

The SLGF is applied at about t=118s, and the feeder breaker opens at about t=118.5s. Before the feeder breaker opens there is a slight voltage rise at the terminal of the 500-kW inverter, maximum of 1.08 PU. Once the island forms, the voltages depress and there is no GFOV observed. The inverters trip in 1.2s, ostensibly from passive-anti-islanding protection.

Table 8. Summary of Tests and Results for Ground Fault Overvoltage on Distribution Feeder/High Side of Inverter Terminal

Test ID	Feeder	Gen/Load ratio	Active Anti-Islanding Enabled?	LVRT Enabled?	Location of Inverter[35]		Trip Time		Maximum Overvoltage Magnitude (PU)	
					1000 kW	500 kW	1000 kW Inverter	500 kW Inverter	Terminal of 1000 kW Inverter	Terminal of 500 kW Inverter
2-9	2	1	No	Yes	A	D	Within 1.2s	Within 0.89s	1.00	1.08
2-10	2	3	No	Yes	A	D	Within 5.4s	Within 5s	2.00	1.94

Figure 24. Plots of Results for Test Case 2-9 Distribution-Side SLGF test with Generation-Load Power Balanced and LVRT Functions Enabled



1) 500kW Inverter output

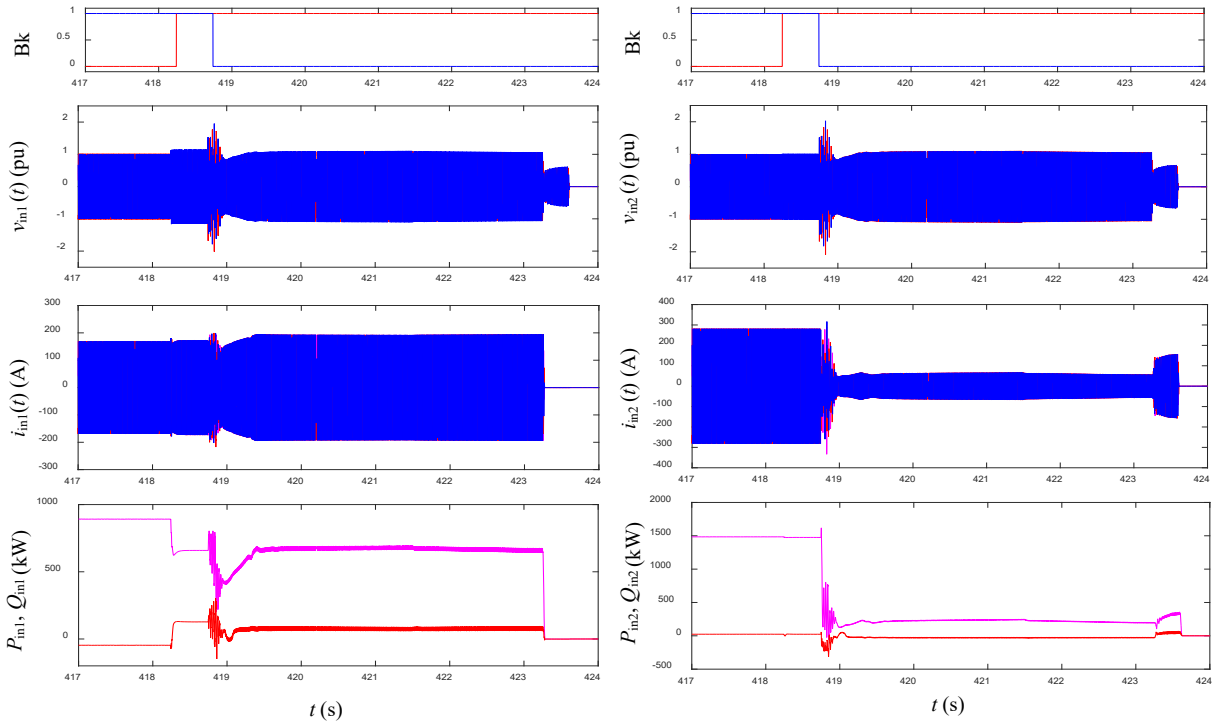
2) 1000kW Inverter output

For test 2-10, the generation is three times that of the load on the island. The plots of test results are shown in Figure 25. Here, GFOV occurs just after the island forms, peaking at 2.0 PU. In response to

the overvoltage, the inverters reduce their output currents. Voltages then drop to within normal range. The duration of the GFOV is very short, less than nine cycles. The test inverters are not able to sustain GFOV on the island.

Though the island remains energized for over 5s, there is no further GFOV. With active anti-islanding enabled, the duration of the island will be within the durations noted earlier in section 3.3.1.

Figure 25. Plots of Result for Test Case 2-12 Distribution-Side SLGF Test with Generation-Load Power Ratio 3:1 and LVRT Functions Enabled



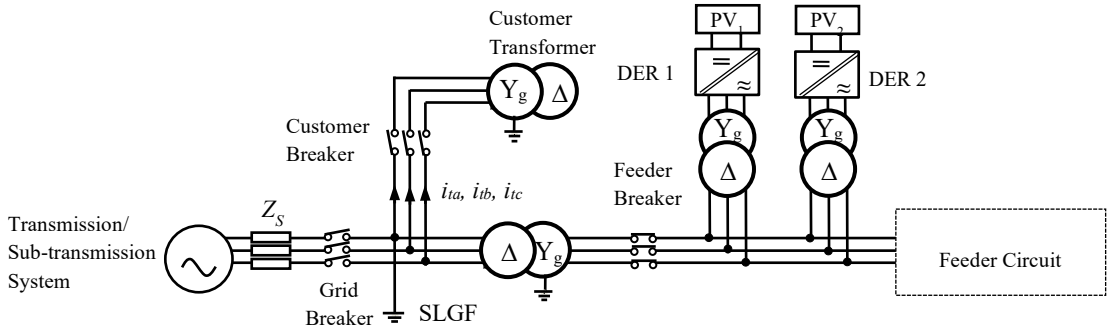
1) 500kW Inverter output

2) 1000kW Inverter output

3.3.4 Ground Fault Over Current

To simulate GFOI on the CHIL setup, the circuit configuration was modified to include an additional transformer representing the alternate grounding source, a customer transformer connected to the subtransmission system. This configuration is shown in Figure 26.

Figure 26. Circuit Diagram of GFOI Test



Inverter active anti-islanding is disabled for this test, so that the results will be generally applicable whether the resulting island is fully balanced or not. The two tests conducted are listed in Table 9.

Table 9. Summary of Tests and Results for Ground Fault Overcurrent

Test ID	Feeder	Active Anti-Islanding Enabled?	Test Conditions	Location of Inverter[36]		3I0 Current (amps)
				1000 kW Inverter	500 kW Inverter	
1-29	1	No	Without alternate grounding source	A	A	0
1-30	1	No	With alternate grounding source	A	A	13.79

The system response for Test Case 1-29 is shown in Figure 27.

- $v_{in1}(t)$ and $i_{in1}(t)$ are the Inverter 1[37] output voltage and current, respectively
- P_{in1}, and Q_{in1} are the Inverter 1 real and reactive power output respectively
- $v_{tD}(t)$ is the substation transformer voltage on the delta side
- $v_{tY}(t)$ is the substation transformer voltage on wye side
- Bk is the triggering signal of grid breaker (blue) and fault breaker (red)
- The zero-sequence current $i_{3I0} = i_{ta} + i_{tb} + i_{tc}$

The SLGF is initiated at t=484.8s. Five cycles later, the grid breaker is opened, islanding the study feeder, the inverters and the fault. GFOV is observed on the subtransmission system on the delta side of the substation transformer as the inverters continue to power the island. Without the alternate grounding source, the current i_{3I0} is zero.

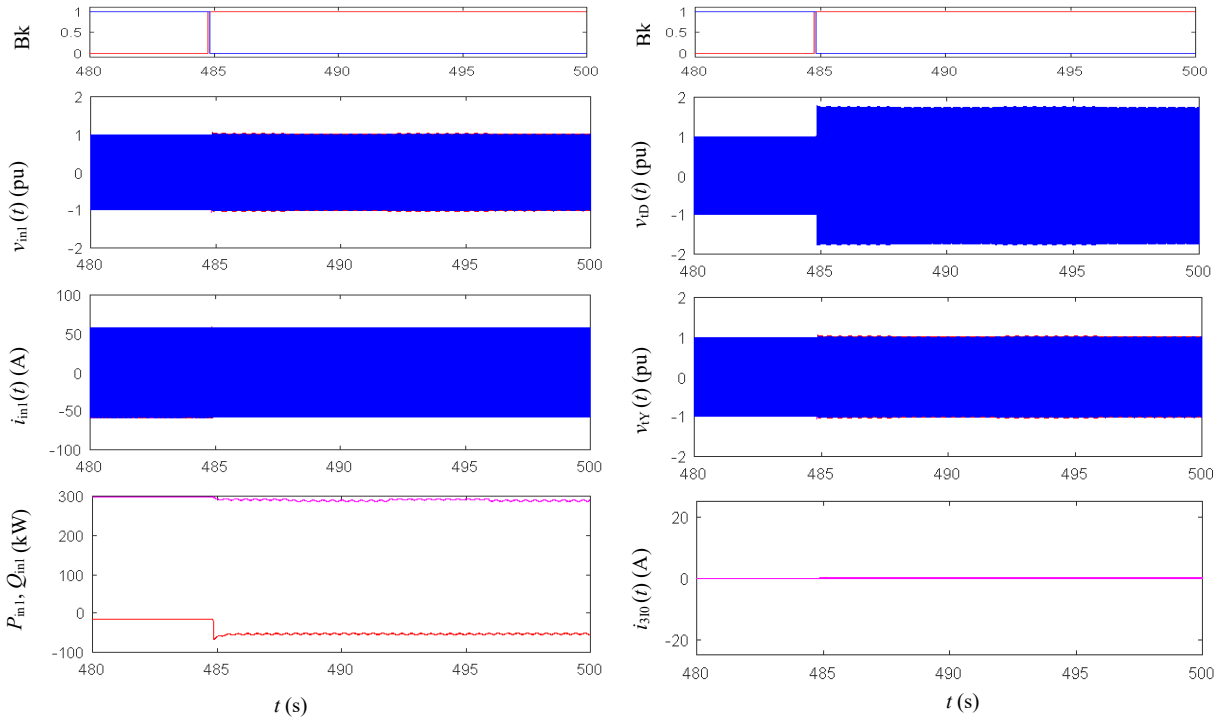
With the alternate grounding source in service (Test Case 1-30), the system response is as shown in Figure 28. The SLGF is initiated at t=550.5s. The grid breaker is switched off five cycles later. There is no ground fault overvoltage any more due to the presence of the alternate grounding source. The

zero-sequence current flowing into the customer transformer has a peak value of about 16 A. The two inverters shut down within 1s from their passive anti-islanding functions.

When there is an alternate grounding source on the same sub-transmission system, GFOV does not occur. The alternate grounding source is generally in the form of a customer transformer with a wye-grounded/delta connection, a three-winding transformer or an autotransformer.

There is a ground fault current that flows in the alternate grounding source. For the simulations, the customer transformer is specified as 2.5 mega-volt ampere (MVA), 69/13.2 kV, connected wye-grounded/delta. The magnitude of the 3I0 current is about 12 amps RMS. Each leg of the transformer winding carries one-third of the neutral current. The customer transformer will have a continuous rating of 3% for 10s (per ANSI/IEEE Std. 32-1972) and a short-term rating which is 33 times the continuous rating, or just under 2100 amps. Note that in this ground fault event, the transformer is expected to carry only a short duration of fault current. There is, therefore, not enough ground fault current to overload the transformer.

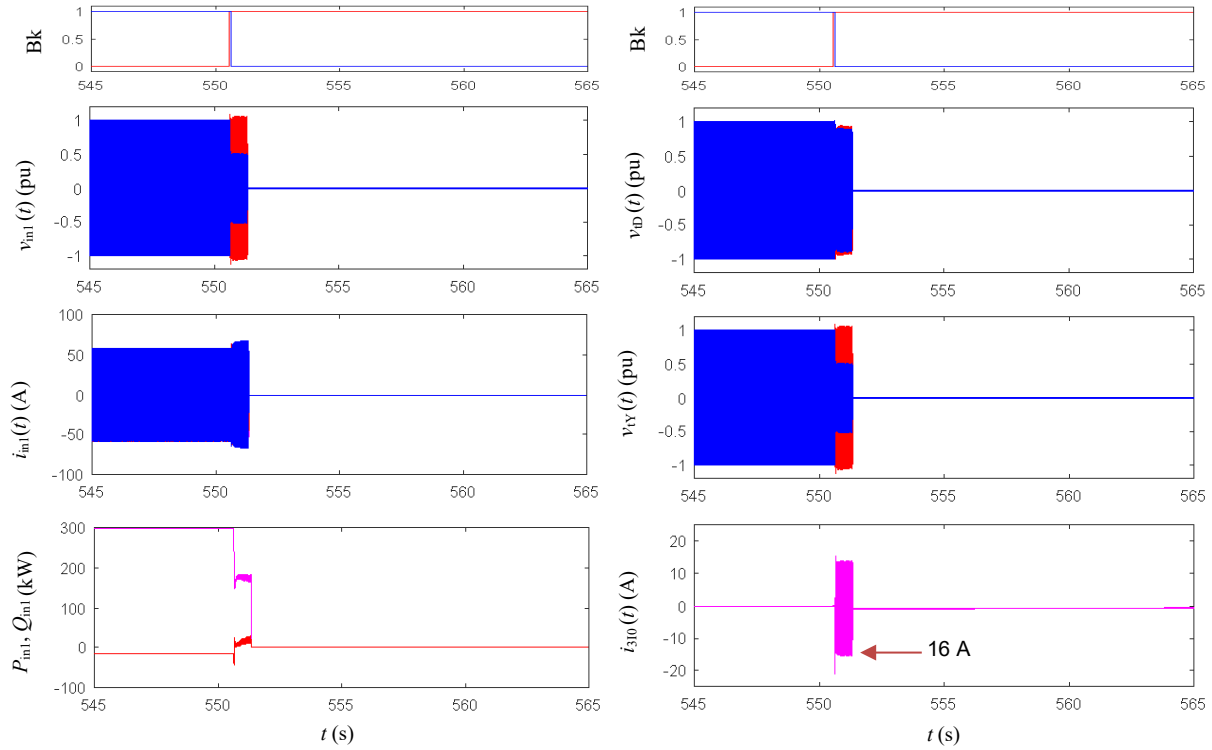
Figure 27. Test Case 1-29: 3I0 Test without Alternate Grounding Source



1) Inverter output

2) Substation transformer voltage & current

Figure 28. Test Case 1-30: 3I0 Test with Alternate Grounding Source



1) Inverter output

2) Substation transformer voltage & current

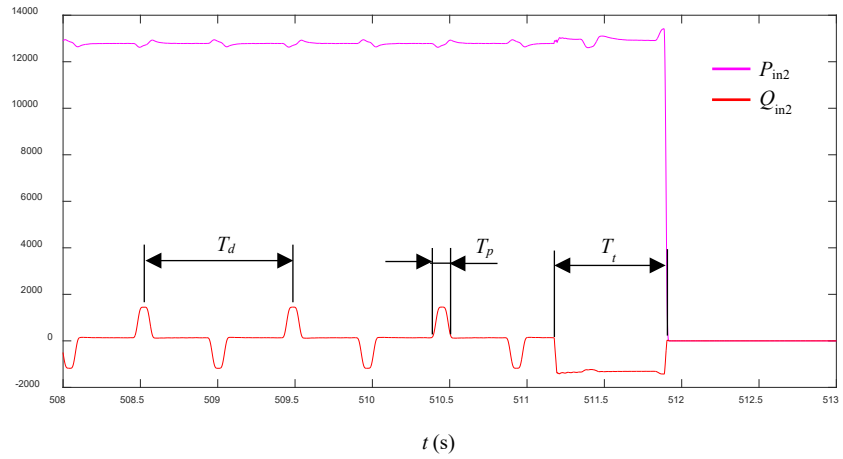
4 Conclusions

To demonstrate the approach and methodology for control-hardware-in-the-loop (CHIL) simulation, three operating distribution feeders were modeled, and two inverter controllers of different ratings were obtained from the manufacturers. These were put together at the test facility at Rensselaer Polytechnic Institute (RPI) and interconnected with the OPAL-RT simulator,[38] a software that enables the key functions of CHIL simulation. The following results and findings are specific to the studied feeders and inverters. Any conclusions inferred herein are specific to the study cases and may not generally be applicable to all feeders and inverters. Non-inverter-based DER may have significantly different response and are not covered in the study.

4.1 Unintended Islanding

Inverters use different methods for active anti-islanding protection. In the study, the inverters introduce an alternating pulse with Pulse duration, T_p, of 0.13s and a period, T_d, of 0.965s. (See illustration below.) Even when two inverters use similar methods for active anti-islanding detection with the same pulse width and period, their response times to an islanding event are dissimilar as evidenced by the different standard deviations of trip time, T_t, between the two inverters used in the tests.

Figure 29. Inverter Pulses from Its Active Anti-Islanding Scheme as Seen in the Real and Reactive Power Output



The inverter trip time is a function of when the islanding occurs in relation to the point in time within the inverter pulse period. If an islanding event occurs immediately after a detection pulse, the inverter takes just a little more time to detect the island compared to an event which occurs just before a pulse. In the case of the of the study inverters, the trip time can vary but remain within a specific number of pulses (i.e., one to two pulses is a time range of 0 to 0.965s, two to three pulses is a time range of 0.483 to 1.448s, and three to four pulses is a time range of 0.965 to 1.93s).

There is an apparent delay in trip time when two inverters are on the feeder compared to when there is only one, but the delay is no more than the time to incur an extra pulse.

For cases with two inverters on the feeder, once the first inverter trips, the remaining inverter trips not only on its own active anti-islanding protection but may also trip on its passive anti-islanding function, since the feeder conditions will now show unbalanced voltage and frequency.

When active anti-islanding is disabled or not available, the inverters fail to trip within 2 seconds. Remedial measures, such as direct-transfer trip (DTT), are needed for this situation. The DTT should initiate on the opening of the feeder breaker and send a trip signal to the inverter(s).

When the study inverters' active anti-islanding protection is enabled, the 1000-kW inverter tends to trip within one to three pulses regardless of feeder type, location in the feeder, or whether or not another inverter is on the feeder. The 500-kW inverter has a slower response requiring at least two pulses and, in some cases, up to four pulses (when two inverters are on the feeder). All the tests conducted had all connected inverters tripping within the 2s limit on response time specified in IEEE Std-1547.

The slower trip times for an inverter apply to certain system conditions including (a) presence of another inverter on the circuit, (b) the inverter is located on the remote end from the feeder breaker, and (c) the inverter is on a feeder with no capacitor bank.

4.2 Ground Fault Overvoltage on the Subtransmission Line

Since a ground fault overvoltage (GFOV) event involves an islanded system, albeit with a single line to ground fault (SLGF), the anti-islanding protection of the inverters can play a role on whether or not the inverters will trip. For the inverters considered in the study, when active anti-islanding is enabled, even

for a fully balanced island, the inverters trip within the same time frame as noted in the islanding test, anywhere from one to four pulses. The time to trip the inverters and de-energize the island can be as much as 1.93s. This duration may be long enough to affect equipment. New York State utilities indicate that this is an unacceptable duration for GFOV as it poses a safety risk to personnel.

The CHIL tests confirm that following the SLGF and formation of the island, voltages as high 1.75 times the pre-event values are observed on the high side of the substation transformer and on the subtransmission system. This is consistent with the all-software simulation (from the Phase 2 Study).

When the active anti-islanding feature is disabled, the inverters do not trip for a fully balanced island, indicating that passive anti-islanding is unable to detect the presence of the ground fault on the subtransmission line. If left undetected, the GFOV can remain active for as long as balanced conditions are present on the island.

Two remedial measures were evaluated. For faster trip times, remedial measures, such as 3V0 and the negative-sequence voltage (NSV) protection schemes, are needed.

- New York State utilities require the implementation of a 3V0 protection. This scheme requires additional equipment and construction at the utility substation that can be expensive for developers of inverter-based generation and will also impose a time delay to their projects. The 3V0 scheme will wait until the sensing relay detects the overvoltage and sends a trip signal to the feeder breakers. This could take as long as six to 24 cycles (0.1 to 0.4 seconds) to occur, just a little bit faster than active anti-islanding protection. In the meantime, the overvoltage remains on the high voltage side.
- For the NSV protection scheme, the response is based on the sequence voltages. Following application of the SLGF, the high side positive sequence voltage drops, while the negative sequence voltage rises. Within a cycle, both the positive and negative sequence voltages reach their target values and stay there until the utility breaker opens. After the breaker opens, the sequence voltages recover to their pre-fault level. The magnitude of incremental change is almost identical in the negative and positive sequence voltage. This response is consistent with simulations discussed in the Phase 2 Report, and thus confirms that the NSV protection scheme will be able to detect the incipient GFOV condition and trip the inverter at a much faster response than the 3V0 scheme.

For the specific inverters tested here, the inverter trip occurs due to the anti-islanding protection. These particular inverters do not detect the overvoltage, unlike some simulation models that were studied previously. Other types and designs of inverters may be able to trip faster by detecting the overvoltage event or by using shorter anti-islanding detection cycles or other forms of anti-islanding protection.

4.3 Ground Fault Overvoltage on the Distribution Feeder

This tests for ground fault overvoltage (GFOV) following a SLGF fault at the inverter terminal. After the SLGF is applied, the feeder breaker opens. This forms an island on the distribution feeder with the fault energized and the inverters online. The concern here is that the voltages on the distribution feeder may show some level of GFOV.

However, the simulations show that no GFOV is observed when the load on the distribution circuit is about the same as the generation. If the load is less than the generation, then there is overvoltage; however, this is very brief (less than nine cycles with generation three times the load on the island) because the inverters reduce output currents in response to the overvoltage. A worst-case scenario is assumed in such a case, where LVRT is enabled and active anti-islanding is disabled.

4.4 Ground Fault Current

When there is an alternate grounding source on the same sub-transmission system, GFOV is not likely to form. The alternate grounding source is generally in the form of a customer transformer with a wye-grounded/delta connection, a three-winding transformer, or an autotransformer.

However, there is a ground fault current (GFC) that flows in the alternate grounding source. For the simulations, a smaller customer transformer is specified in order to determine if it can withstand the incoming GFOI. The magnitude of the 3I0 current in the transformer is less than its continuous rating per ANSI/IEEE Std. 32-1972 and significantly less than the short-term rating. There is, therefore, not enough ground fault current to overload the transformer.

No mitigation is required since the transformer can withstand the GFC in this scenario.

Endnotes

[1] A commercial product of OPAL-RT Technologies.

[2] A commercial product of OPAL-RT Technologies.

[3] For the report, visit http://documents.dps.ny.gov/public/Common/ViewDoc.aspx?DocRefId=BB4B461D-FF72-495F-9B50-8BC82303D7B8 on the New York State Department of Public Service (DPS) Interconnection Technical Working Group (ITWG) website.

[4] "Protection of a transmission side ground fault overvoltage on power transformer equipment from any source on the secondary side will, depending on the protection schemes in place at any substation, require ground fault (or zero sequence) overvoltage ("3V0") protection equipment." National Grid's Technical Review of Pterra Consulting's Report R149-16 "Assessment of Inverter-based Distributed Generation Induced Ground Fault Overvoltage on Delta-Wye Substation Transformers", January 31, 2017, posted on ITWG webpage and accessible via this link.

[5] 3V0 comes from the fact that the zero-sequence voltage, V0, needs to be multiplied by three to permit the measurement.

[6] Pterra Consulting Report, "Assessment of Inverter-based Distributed Generation Induced Ground Fault Overvoltage on Delta-Wye Substation Transformers", January 3rd, 2016 available at this link.

[7] Pterra Consulting Presentation Slides, "Assessment of Inverter-based Distributed Generation Induced Ground Fault Overvoltage on DeltaWye Substation Transformers", January, 2016 available at this link.

[8] Tom Short, "Application for IEEE C62.92.6-2017, NY DPS ITWG Meeting, Albany, NY, August 29, 2018, available at this link.

[9] For the report, visit http://documents.dps.ny.gov/public/Common/ViewDoc.aspx?DocRefId=BB4B461D-FF72-495F-9B50-8BC82303D7B8 on the New York State Department of Public Service (DPS) Interconnection Technical Working Group (ITWG) website.

[10] Essential findings of the report are presented in PowerPoint format. Visit http://documents.dps.ny.gov/public/Common/ViewDoc.aspx?DocRefId=%7B583C0024-9121-472B-8EA5-491107F5DEFB%7D on the New York State Department of Public Service (DPS) Interconnection Technical Working Group (ITWG) website.

[11] MATLAB/Simulink is a commercial product of Mathworks

[12] A commercial product of OPAL-RT Technologies.

[13] NYSEG is New York State Electric & Gas, a wholly-owned subsidiary of AVANGRID, Inc.

[14] For confidentiality reasons, the name of the manufacturer is withheld.

[15] Seven digital output (DO) ports and 15 analog input (AI) ports

[16] Field-programmable gate array, a type of integrated circuit

[17] At the time of the study, the 32-core Real-time SuperServer simulator was not available.

[18] Both real and reactive power is balanced.

[19] "Fully-balanced" here means balanced three-phase loading such that all three phase currents into the breaker that initiates the islanding event are zero.

[20] See Section 2.3 for further discussion.

[21] Inverter 2 is rated 1000 kW. Please refer to Table 2 for further specifications.

[22] These are percent of the time that the trip time is below the stated values.

[23] Inverter 1 is rated 500 kW while Inverter 2 is rated 1000 kW. Please refer to Table 2 for further specifications.

[24] A = Near the feeder breaker, D = remote end from the breaker. Locations B and C are at intermediate locations.

[25] 1-2 pulses is a time range of 0 to 0.965s; 2-3 pulses is a time range of 0.483 to 1.448s, and 3-4 pulses is a time range of 0.965 to 1.93s.

[26] This is the same as Test Case S-1.

[27] This is the same as Test Case S-2.

[28] A pulse is 0.483s long. This is specific to the study inverters.

[29] Inverter 2 is rated 1000 kW. Please refer to Table 2 for further specifications.

[30] A = Near the feeder breaker, D = remote end from the breaker. Locations B and C are at intermediate locations.

[31] 1-2 pulses is a time range of 0 to 0.965s; 2-3 pulses is a time range of 0.483 to 1.448s, and 3-4 pulses is a time range of 0.965 to 1.93s.

[32] See Section 1.3.5.

[33] Note that between the location of the SLGF on the high side and the terminal of the inverter on the low side, there is delta-wye transformer.

[34] Inverter 2 is rated 1000 kW. Please refer to Table 2 for further specifications.

[35] A = Near the feeder breaker, D = remote end from the breaker. Locations B and C are at intermediate locations.

[36] A = Near the feeder breaker, D = remote end from the breaker. Locations B and C are at intermediate locations.

[37] Inverter 2 is rated 1000 kW. Please refer to Table 2 for further specifications.

[38] A commercial product of OPAL-RT Technologies.

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